

Model Name: GA-Z170X-SOC Force

Rev 1.01

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B
06	CPU_LGA1151-C
07	CPU_LGA1151-D
08	DDR III CHANNEL A
09	DDR III CHANNEL B
10	PCH_DP,CLK BUFFER
11	PCH_FDI,DMI,USB,PCIE
12	PCH_GPIO,MISC
13	PCH_SATA,PCIE,SATA_EXPRESS
14	PCH_PWR,GND
15	PCI EXPRESS*1 SLOTS X3
16	ALC1150
17	Audio Connect,AMP
18	I/O ITE8628
19	Audio Power,LED
20	FP,TPM,BZ
21	80 PORT
22	DISCRETE POWER
23	NCT3933
24	IDT6V41510_CLK BUFFER
25	ATX POWER
26	INTEL I219
27	LAN CONNECTOR
28	IT8951
29	IT8792
30	FAN CTRL
31	Dual BIOS
32	PEX8747S UPSTREAM & MISC
33	PEX8747S DOWNSTREAM SLOTS
34	PEX8747S STRAP & CPLD INTF
35	PEX8747S POWER
36	PEX8747 POWER DESIGN
37	PCI EXPRESS*16_1 SLOT
38	PCI EXPRESS X16 SWITCH_1
39	PCI EXPRESS*8_1 SLOT
40	PCI EXPRESS*16_2 SLOT
41	PCI EXPRESS X16 SWITCH_2
42	PCI EXPRESS*8_2 SLOT
43	DVI
44	DP PORT
45	RENESAS USB3 HUB-1

SHEET

TITLE

46	RENESAS USB3 HUB-2
47	F_USB3.0
48	F_USB2.0
49	KB/MS/USB2.0
50	IR3570_DDR PWM
51	IR3553_DDR MOS
52	IR3553_VPP MOS
53	VCCPLL
54	IR3580-VCORE PWM
55	IR3553-VCORE MOS-1
56	IR3553-VCORE MOS-2
57	IR3553-VCORE MOS-3
58	IR3553-VCORE MOS-4
59	IR3580-VCCGT PWM
60	IR3553-VCCGT MOS
61	RT8120_PCH POWER
62	R_USB3.0
63	IR3570_VSA PWM
64	IR3553_VCCSA MOS
65	IR3553_VCCIO MOS
66	ASM106SE-SATA EXPRESS
67	OC_PANEL
68	OC_BUTTON-1
69	OC_BUTTON-2
70	COM,Thunderbolt PIN
71	PCIE SW
72	M2-1
73	M2-2
74	SATA_PRESS-2
75	M2 SWITCH-2
76	M2-3
77	SATA_PRESS-3
78	M2 SWITCH-3
79	EMI-ESD
80	HS
81	ALPINE RIDGE CIO & DP
82	ALPINE RIDGE POWER
83	U3.1 PORT A
84	HD3SS321&TUSB321_A
85	HDMI
86	CPU POWER1
87	NTC

88 TABLE LIST

Gigabyte Technology

Title		Cover Sheet	
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date	Wednesday, September 30, 2015	Sheet	1 of 88

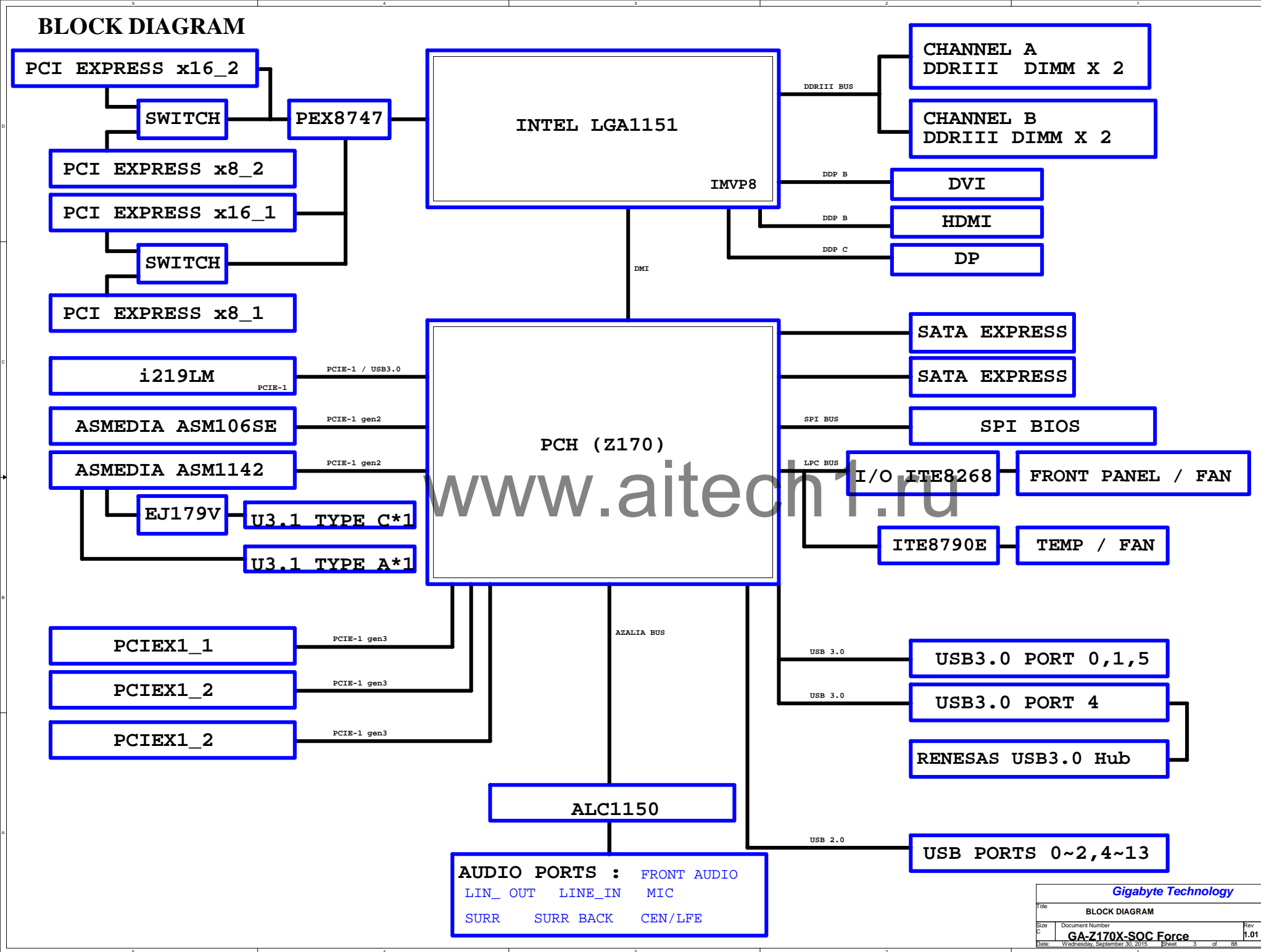
GA-Z170X-SOC Force
Component value change history

[illegible][illegible]

Circuit or PCB layout change

DATE	Change Item	Reason
2015/01/14	NEW	0.1b
2015/04/20	1.修改JVDUAL and JVDUAL_PCH 網路 2.修改xio網路,ADD OR94.Q05 3.修改SHORT PAD 4.DSEL=LABEL1 5.MC01FF=LABEL1(220/S)-->(100/S),LABC29(220S)-->(100/S/X) 6.ADD=LABC5,LABC6(499/4/1) M0 JVDUAL_LAN1 7.LAYOUT注意:LABC32,LABC29 CLOSE LAG1,LABC10 CLOSE PINA 8.LABC25=short pad 9.Remove HDMI2.0 CHIP .AEM142 10.ADD Alpine Ridge 11.修改dual xio-on網路 12.OC_PANEL remove	0.11b
2015/05/29	1.修改ASML06:模組網路+3B+ADD REPRCH 2.修改CPL Buffer:模組網路:0B+模組背板網路 3.LAN 1219模組網路:5.599 ADD LAG1.LQ1 4.修改NR22,PNR8 Footprint 5.修改CCH 模組網路:7B Remove NR294,NR295 6.ADD NR324,NR325,NR326 7.改HKEY PAD 8.修改DUAL1:線路模組0.41b+TYPE C改使用RJ179b+RJ179D	0.2b
2015/07/14	1.Remove "NR22" , VDDSPD --> VPP25V 2.ADD DM_SBC1, DM_SBC2, DM_SBC3, DM_SBC4, DM_SBC5, DM_SBC6, DM_SBC7,DM_SBC1 (CPU背板電容) 3.修改CPU模組 remove TR3,TR2 4.修改SIO 模組 +ADD OR170 5.修改CCH POWER 模組 +ADD NP010 . NP022改005	0.3b
2015/07/30	DDR改CIP	1.0b
2015/08/14	1.Add M_OVC9 - M_OVC10 2.Remove NR300,NR301,NR102,NR103 3.Remove NR302,NR303+直接接CPU 4.Remove NR110,NR112+直接接CPU	1.01b

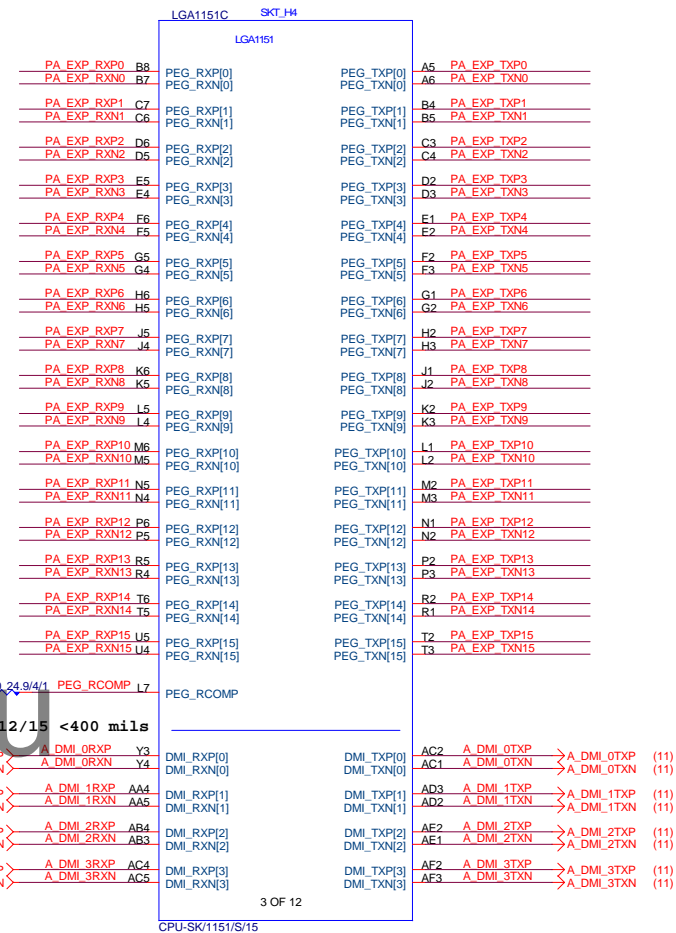
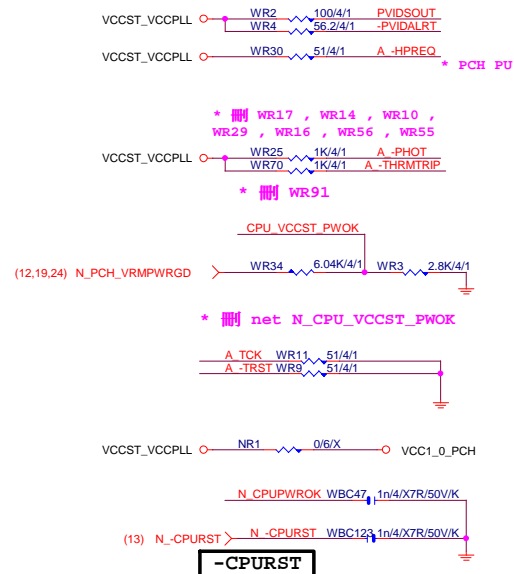
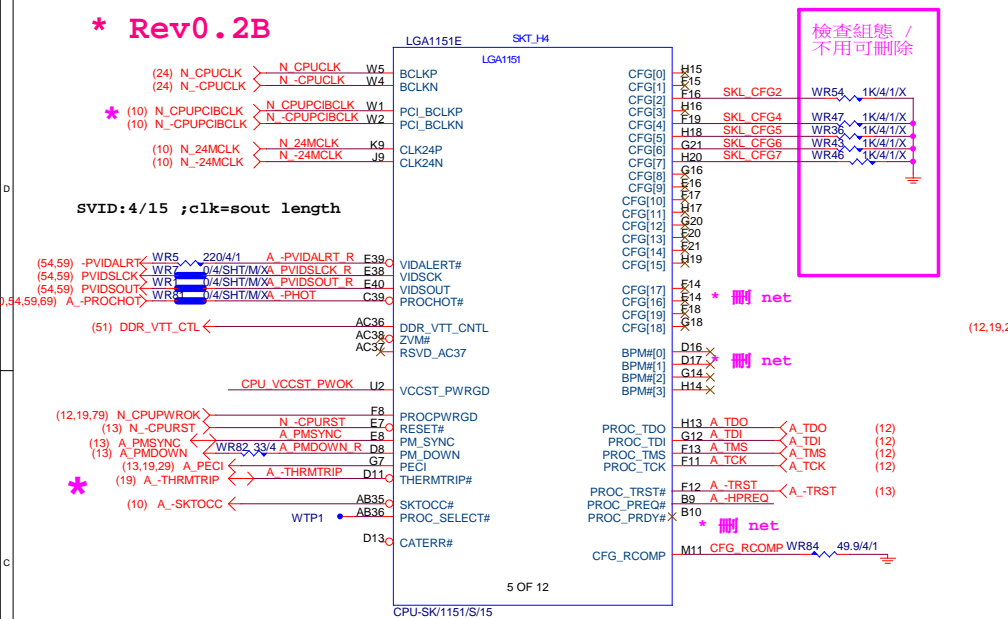
BLOCK DIAGRAM



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BLOCK DIAGRAM		
Size	Document Number	Rev
C	GA-Z170X-SOC Force	1.01
Date:	Wednesday, September 30, 2015	Sheet 3 of 88

* Rev0.2B



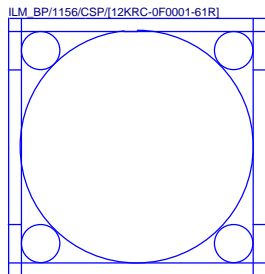
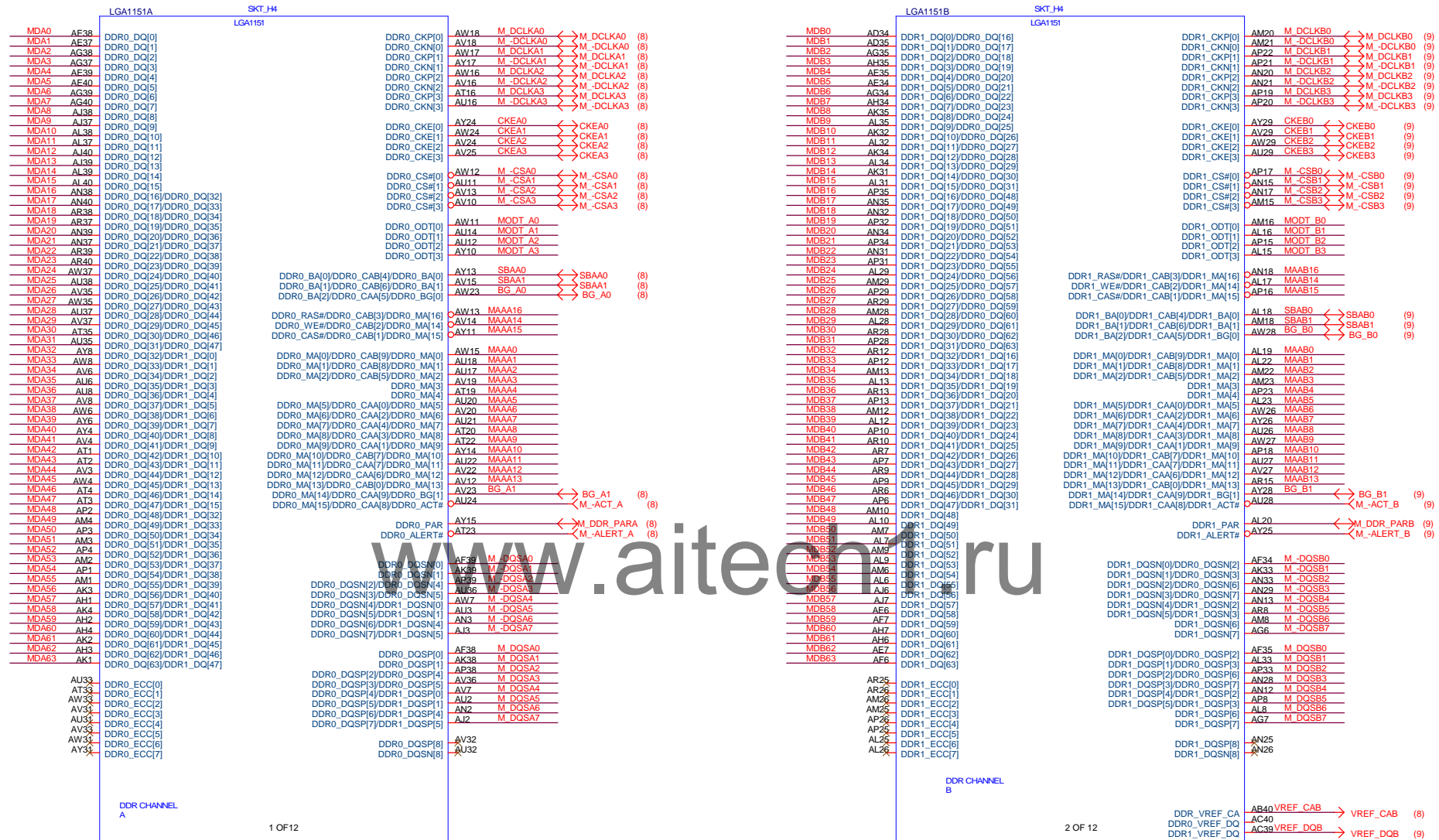
```
CFG[2]:x16 Lane Numbering
Reversal. 1= NORMAL;0=reversal
CFG[4]: eDP
enable:1:disable/0=enable
CFG[6:5]:PCI Express* Bifurcation: 11=
1 x16 PCI Express;10=2x8 PCI Express
CFG[7]: PEG Training:1=(default) PEG Train
immediately following RESET*;0=PEG Wait for BIOS
```

Bifurcation Config.	Signals Lanes		
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
4x4+2x4	0	0	1
1x8+2x4 Reversed	0	0	0

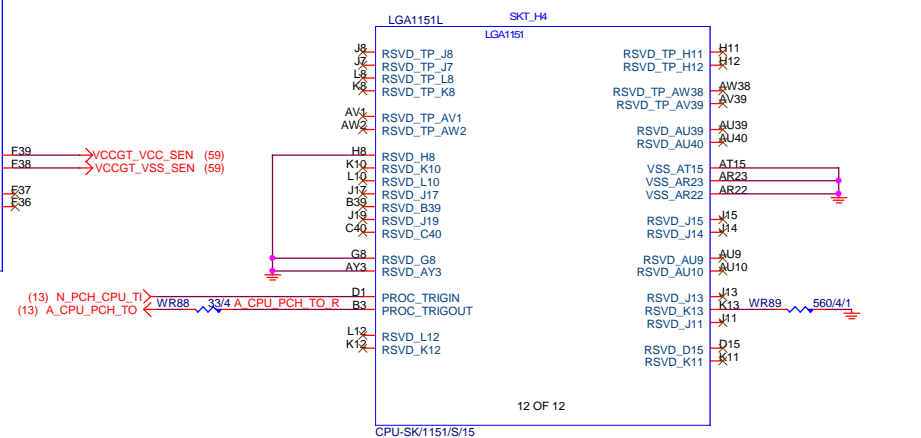
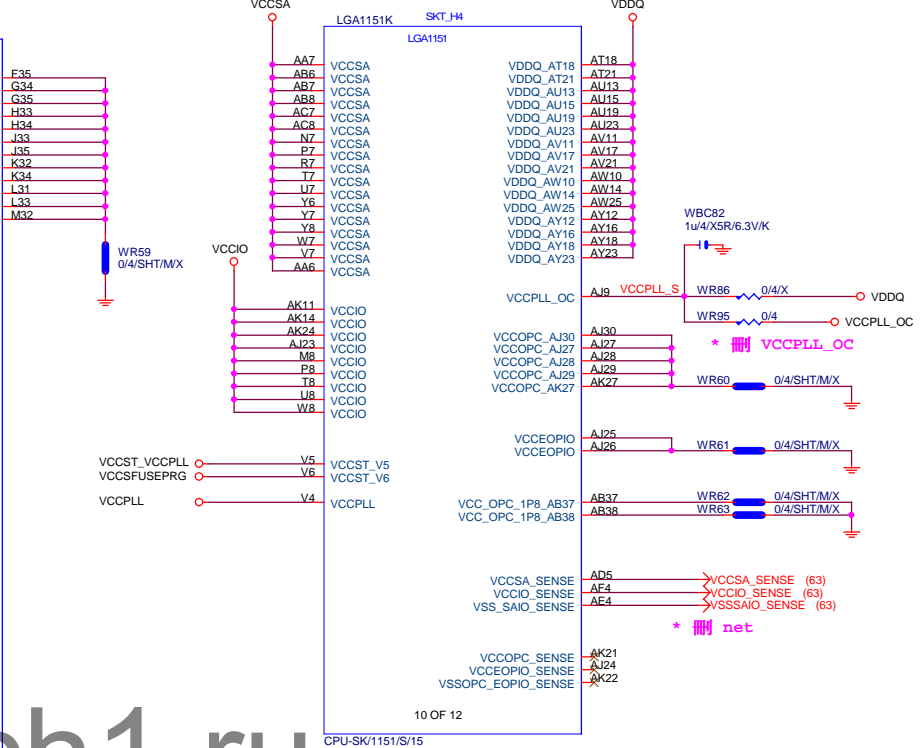
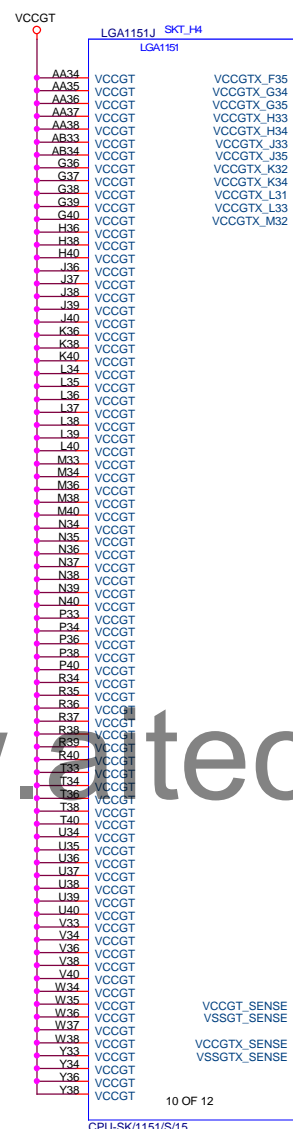
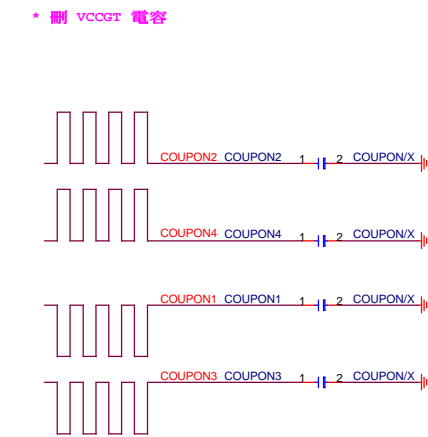
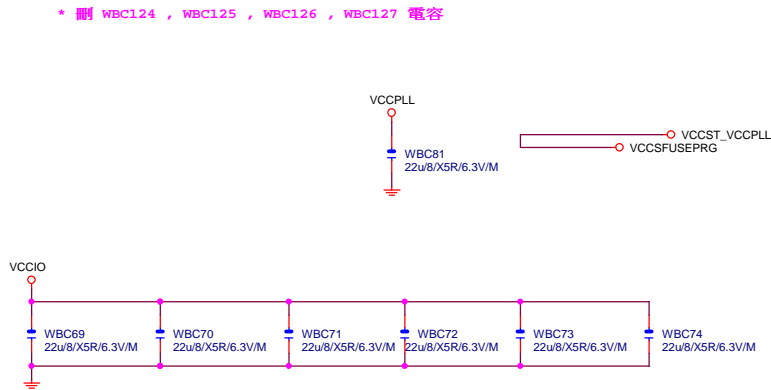
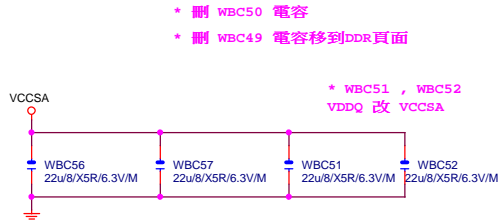
PA EXP TXP[0..15] >> PA_EXP_TXP[0..15] (32)
PA EXP TXN[0..15] >> PA_EXP_TXN[0..15] (32)
PA EXP RXP[0..15] >> PA_EXP_RXP[0..15] (32)
PA EXP RXN[0..15] >> PA_EXP_RXN[0..15] (32)

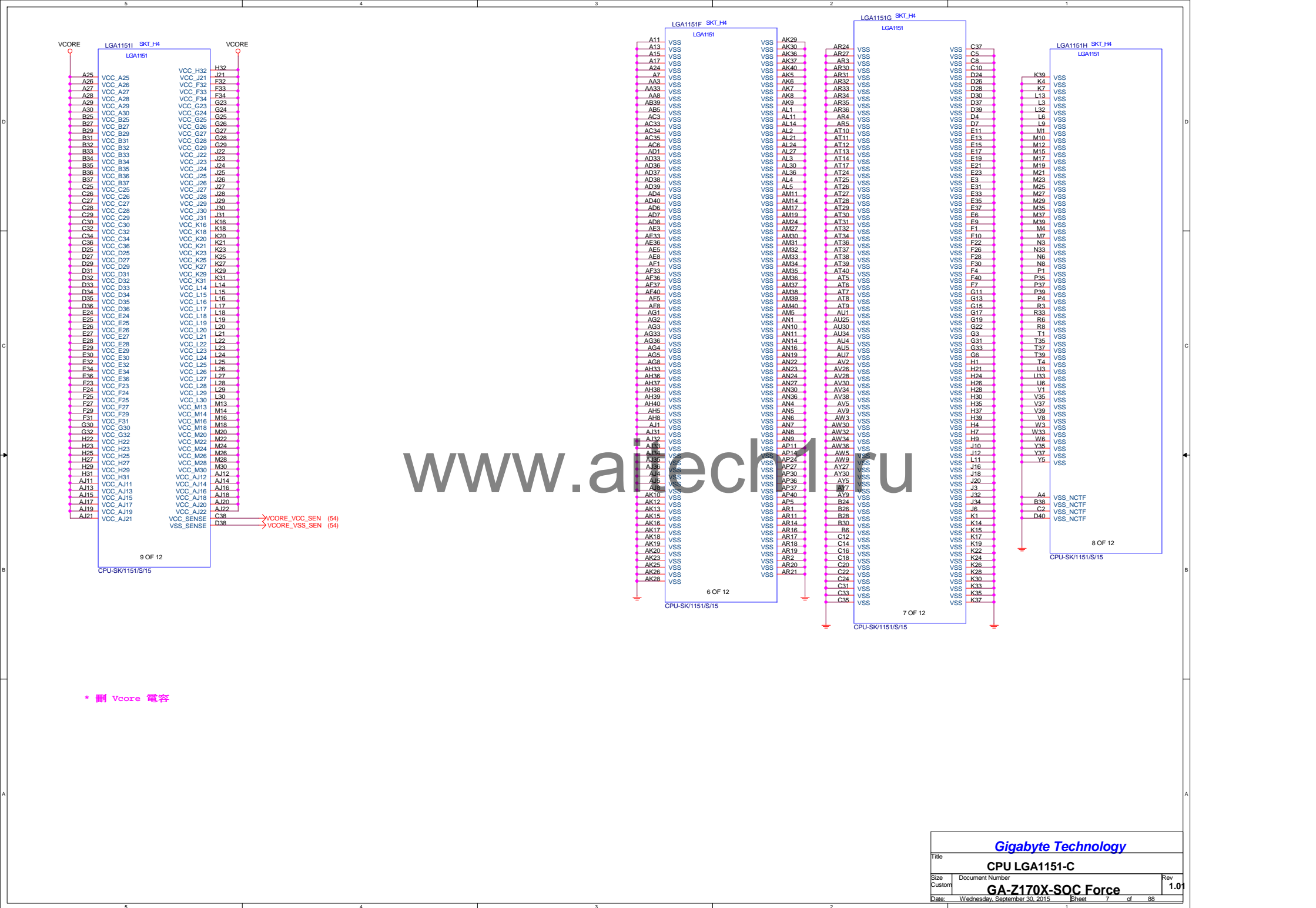
```
4 layer PEG/DMI=====4/4/4//15
6 layer PEG/DMI=====4/5.5/4//15
-----
Impedance=85 +- 15%
```

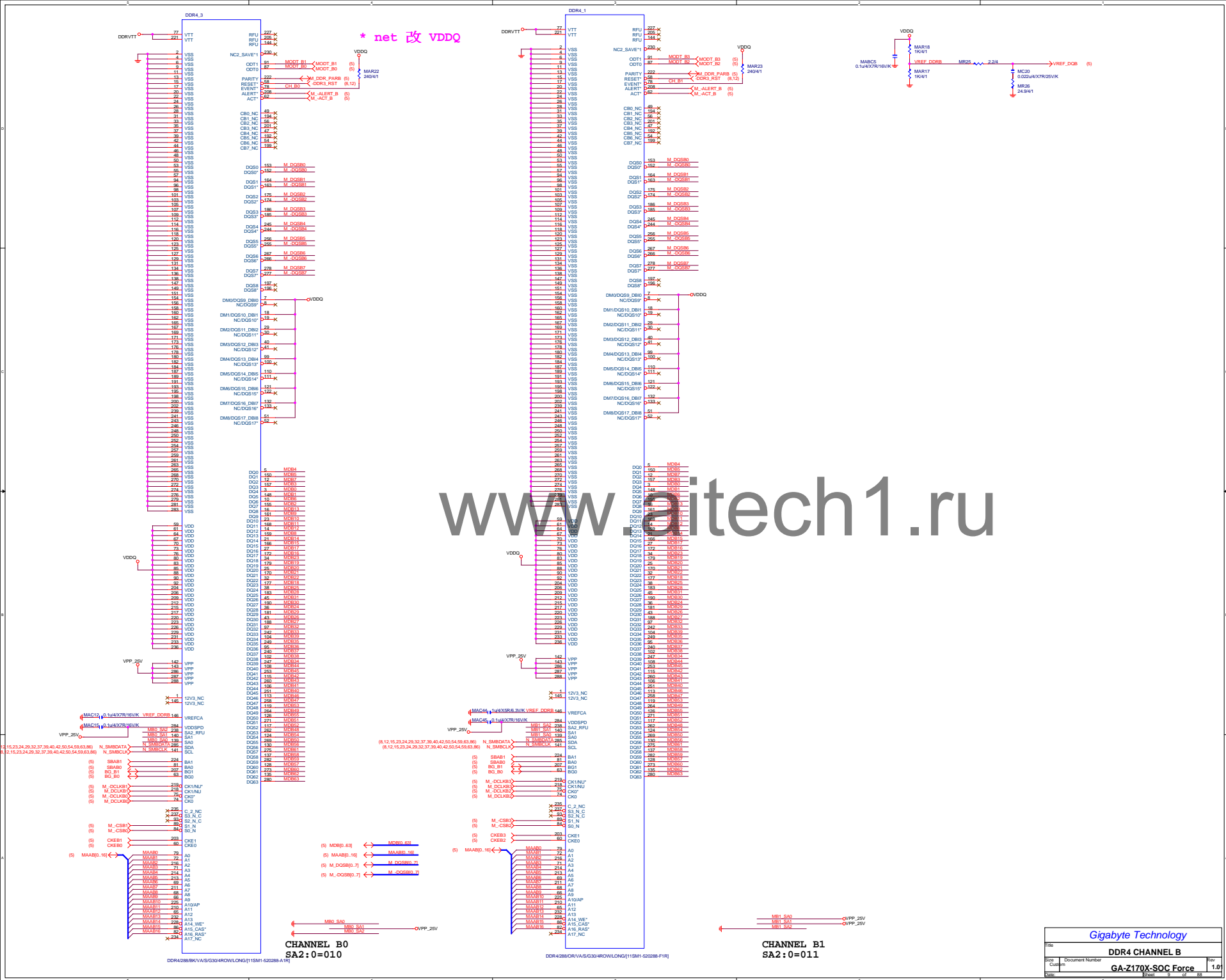

* 改DDR4 net

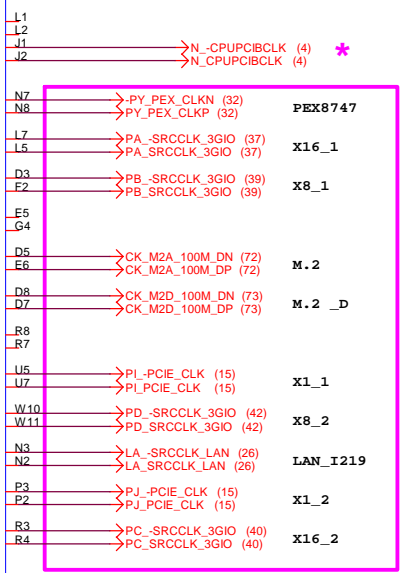
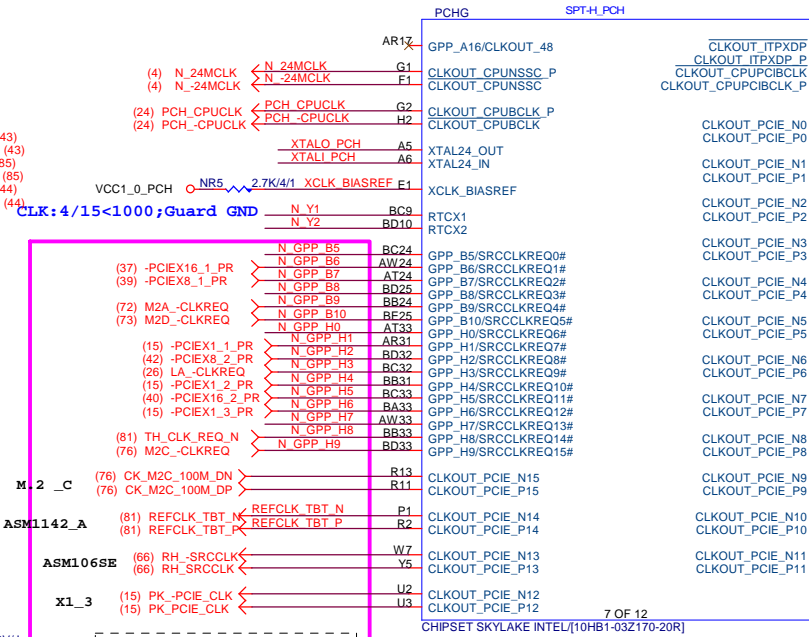
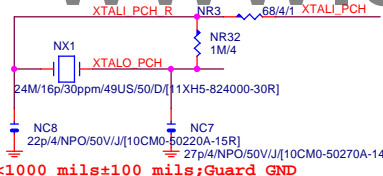
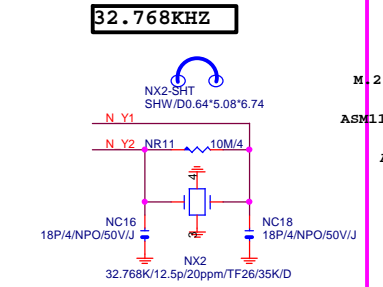
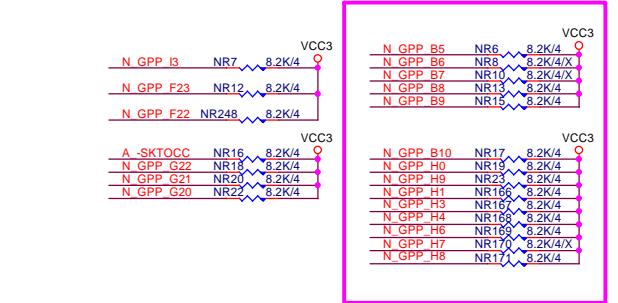
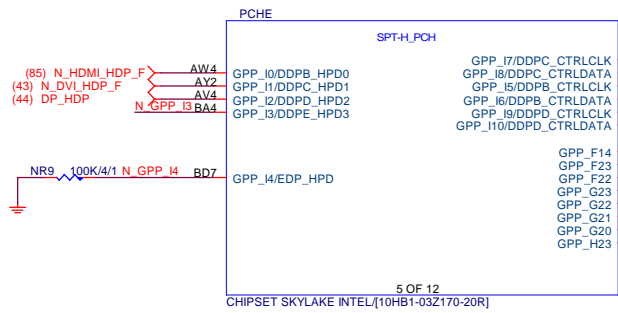


Need check the new CPU ME



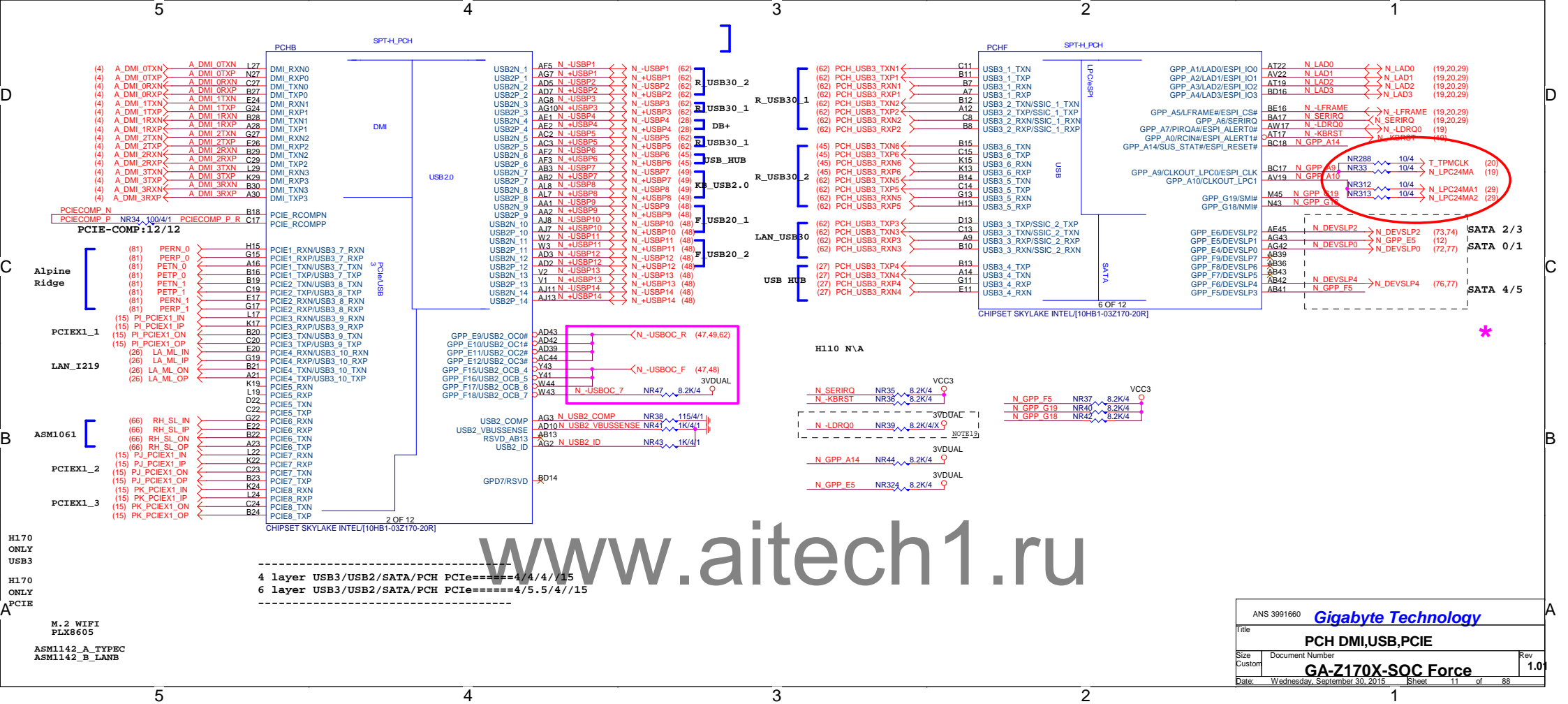






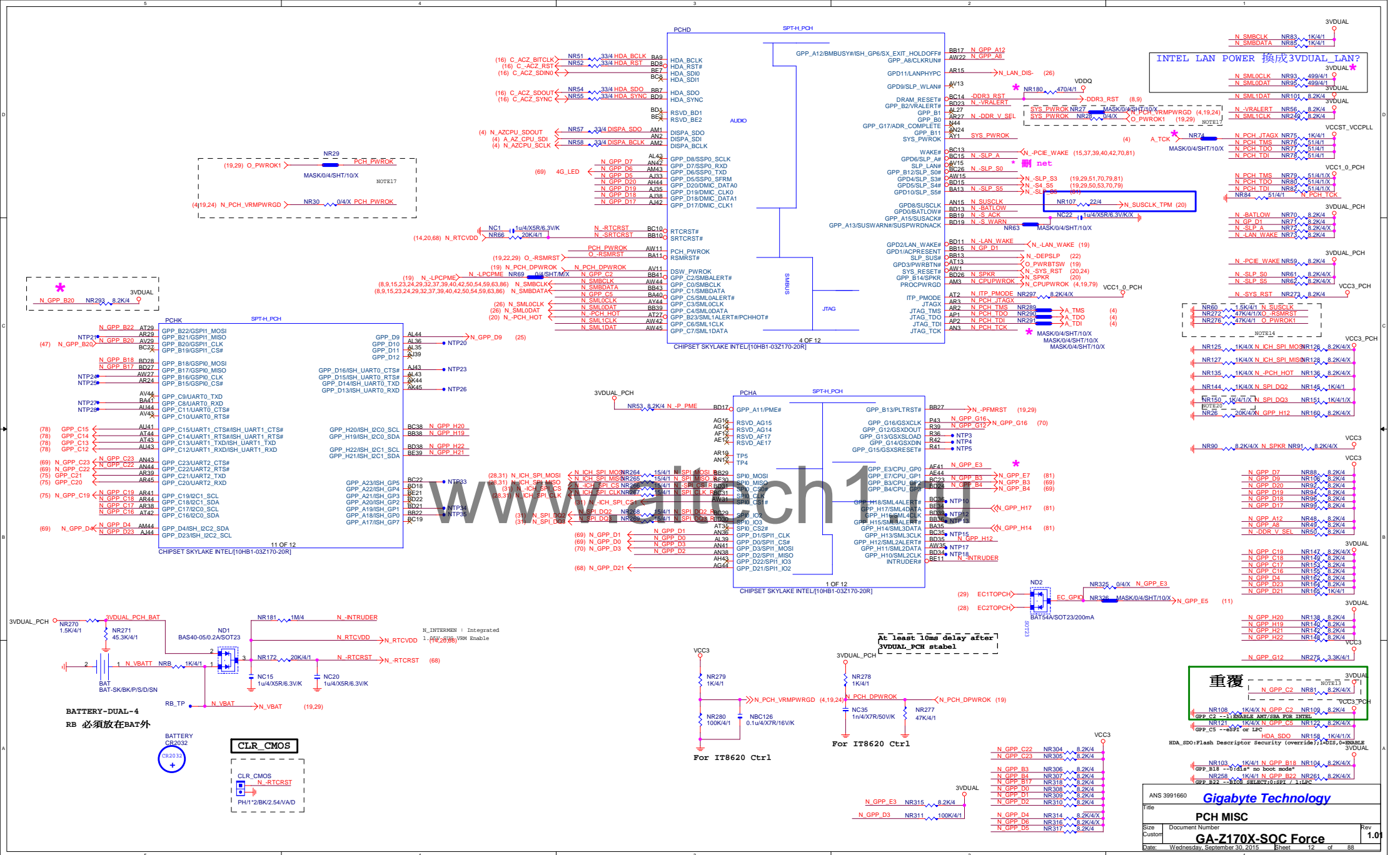
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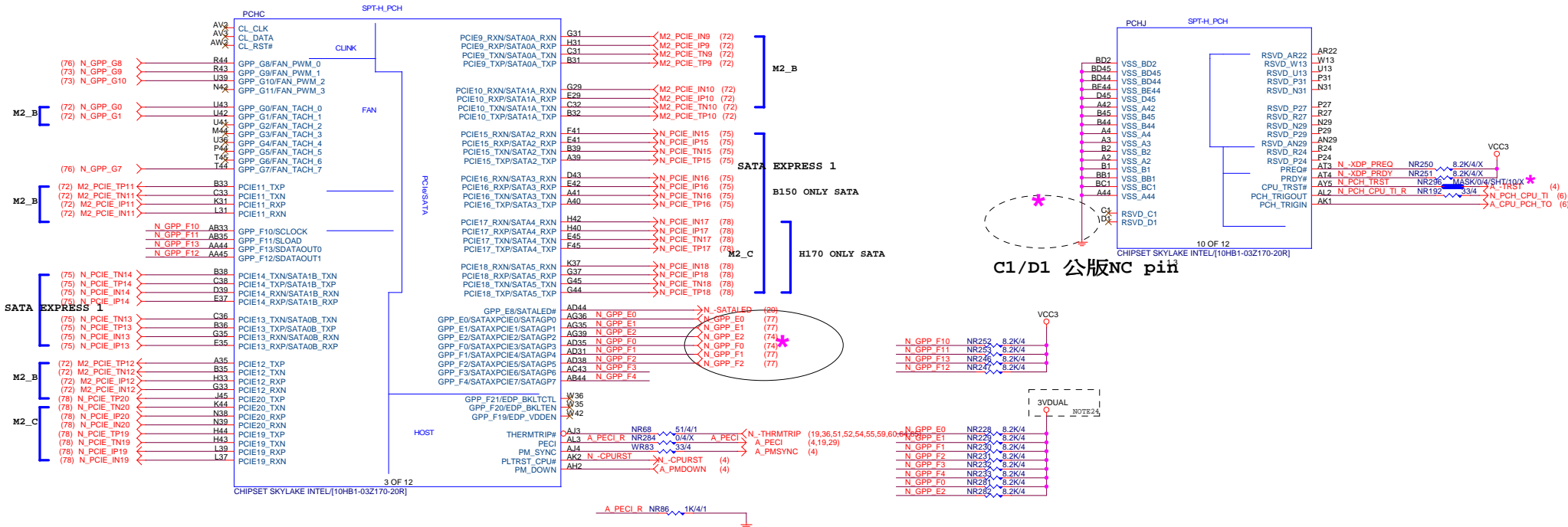
ANS 3991660		Gigabyte Technology	
Title			
PCH CLOCK BUFFER			
Size Custom	Document Number		Rev 1.01
GA-Z170X-SOC Force			
Date:	Wednesday, September 30, 2015	Sheet 10 of 88	



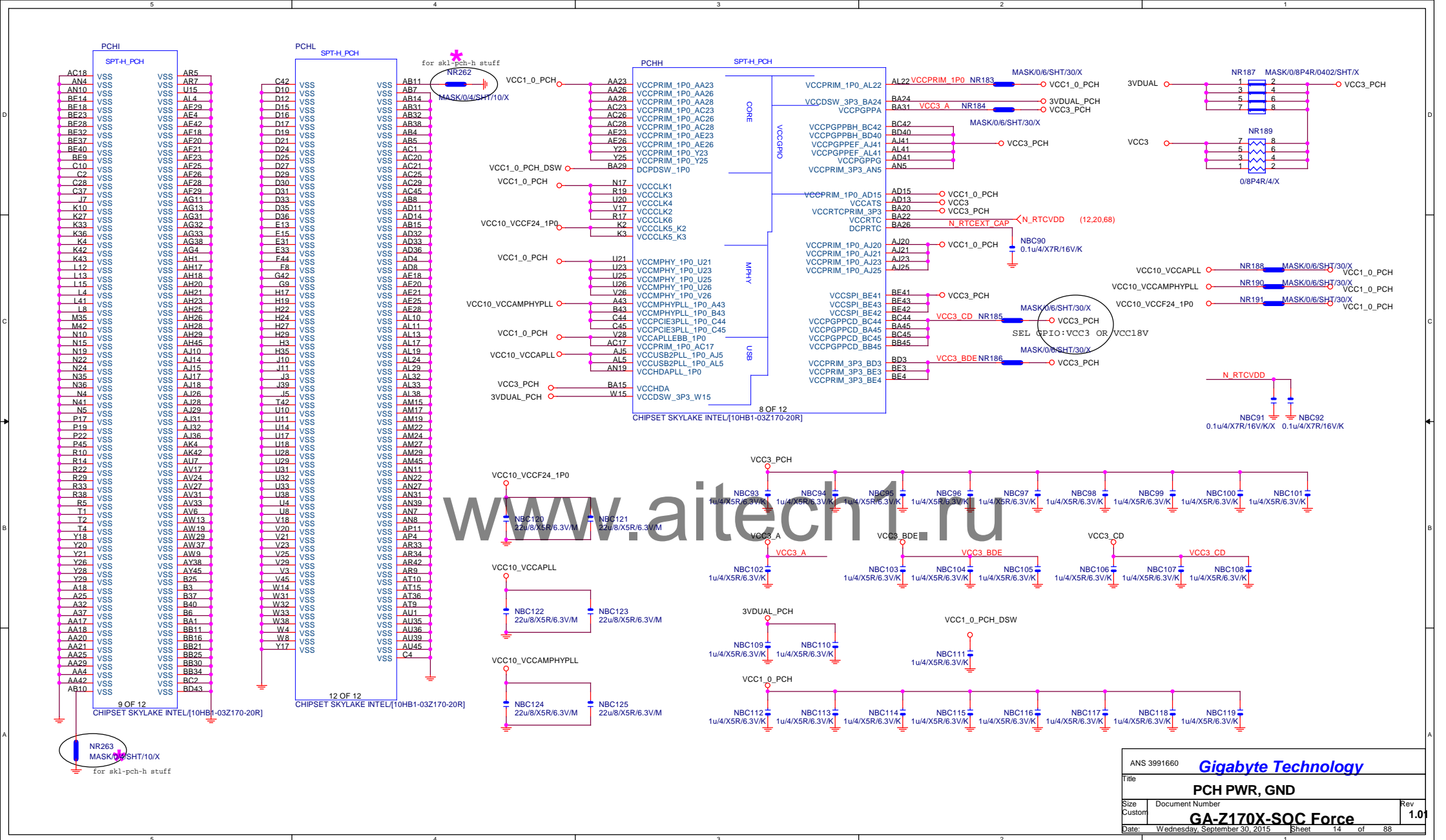
4 layer USB3/USB2/SATA/PCH PCIe=====4/4/15
6 layer USB3/USB2/SATA/PCH PCIe=====4/5.5/4/15

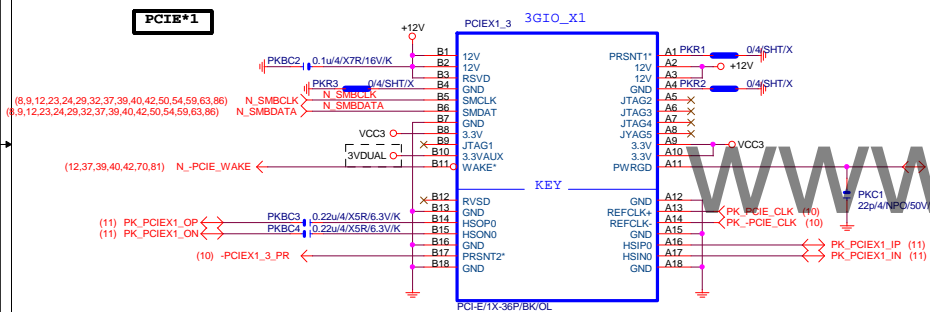
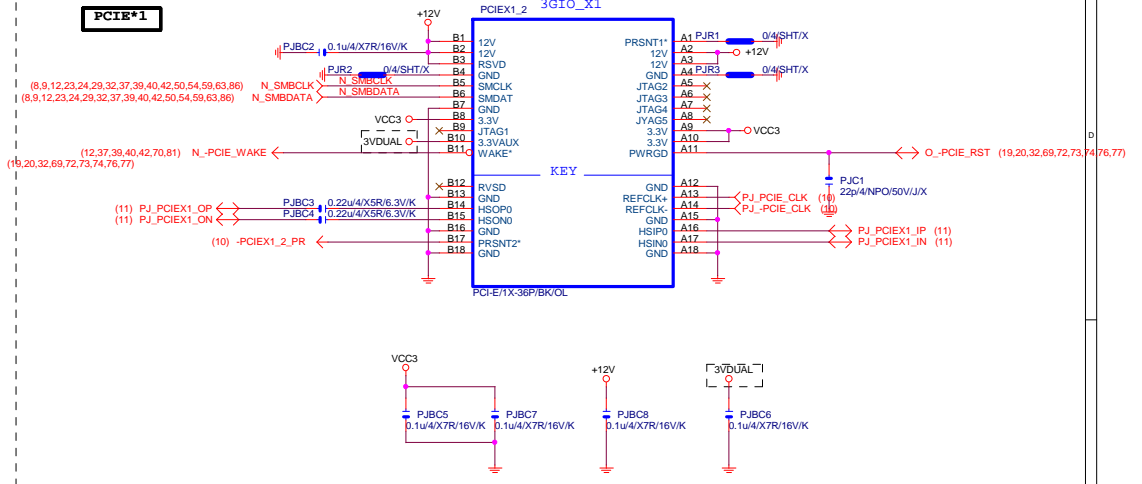
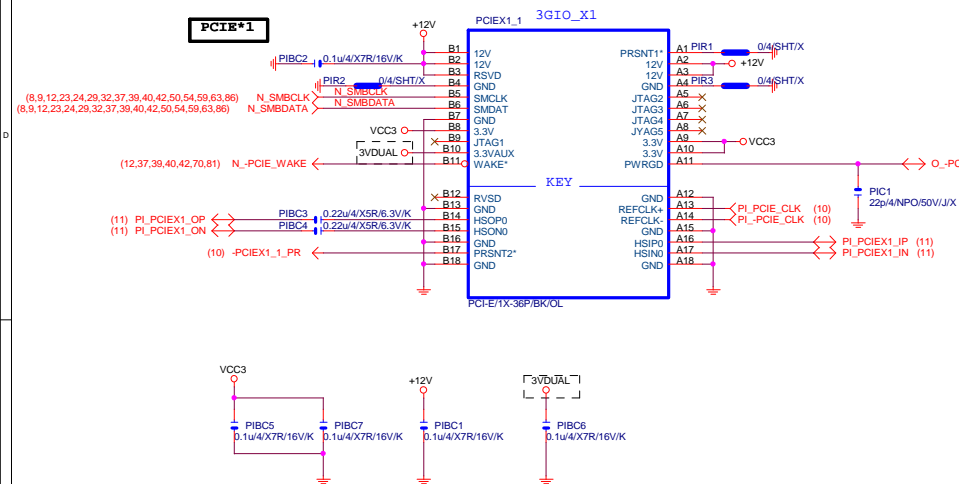
ANS 3991660		Gigabyte Technology	
Title		PCH DMI,USB,PCIe	
Size	Document Number	Rev	1.0
Customer		GA-Z170X-SOC Force	
Date:	Wednesday, September 30, 2015	Sheet	11 of 88





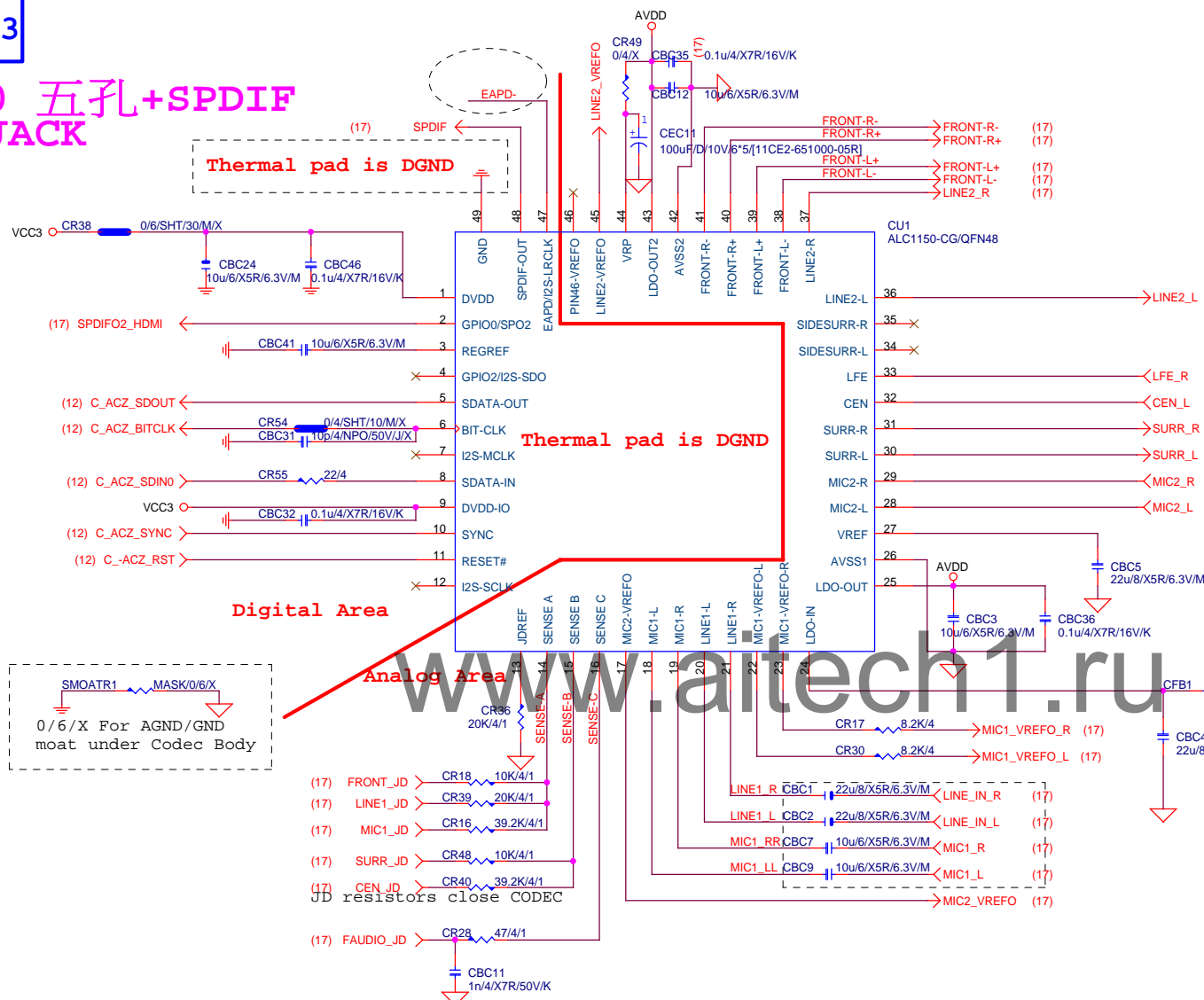
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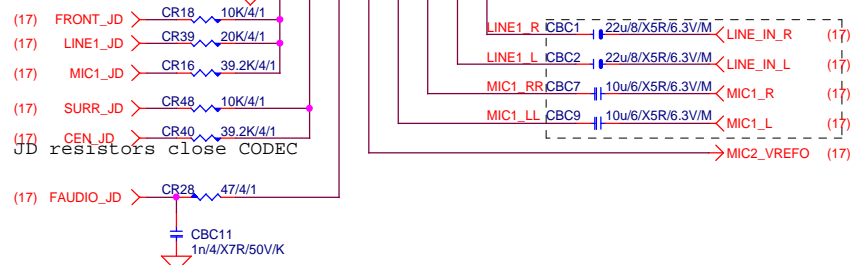
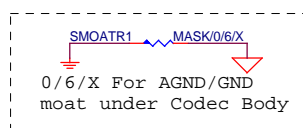
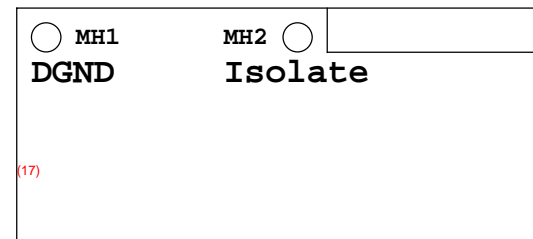


Rev 0.93

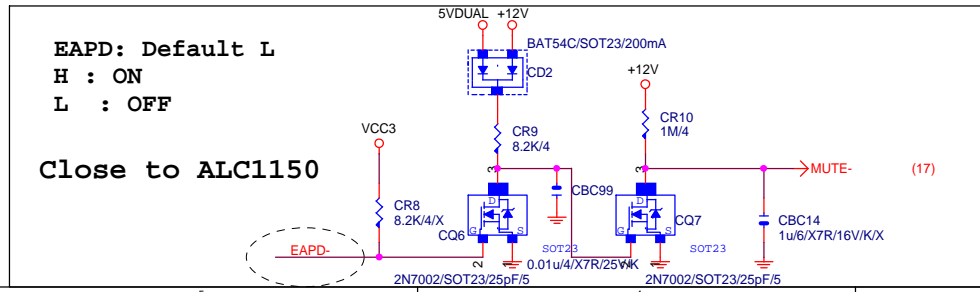
ALC1150 五孔+SPDIF AUDIO JACK



LAYOUT注意:螺絲孔下GND方式
1. MH1空間夠,下DGND
空間不夠,改為Isolate
2. MH2一律改為Isolate

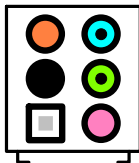


LAYOUT注意:要加
GND切割線

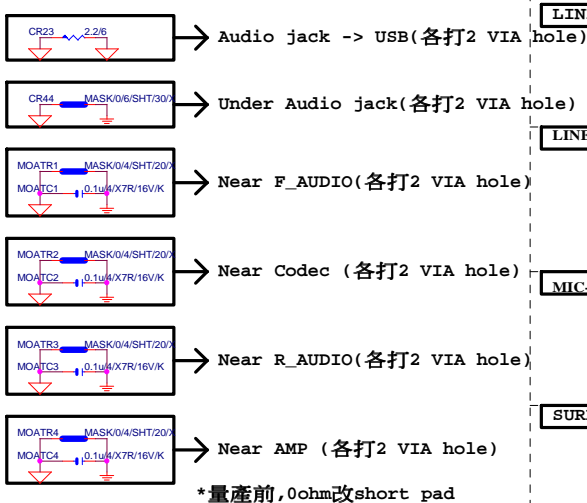
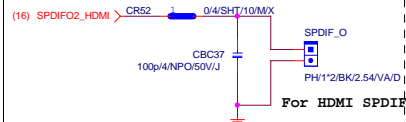


Gigabyte Technology			
Title			
ALC1150			
Size	Document Number	GA-Z170X-SOC Force	
Custom		Rev 1.01	
Date:	Wednesday, September 30, 2015	Sheet	16 of 88

AZALIA JACK

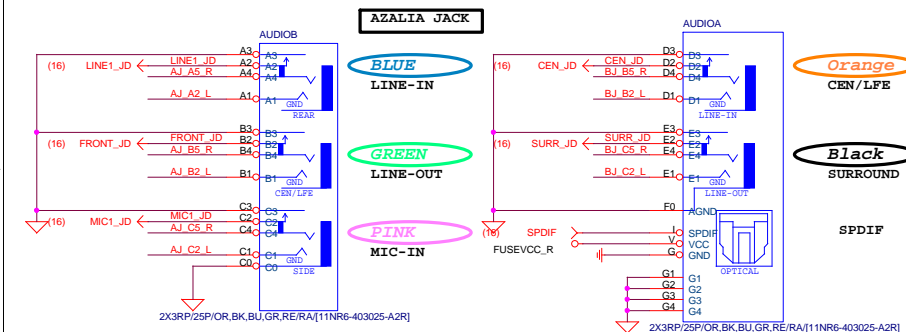
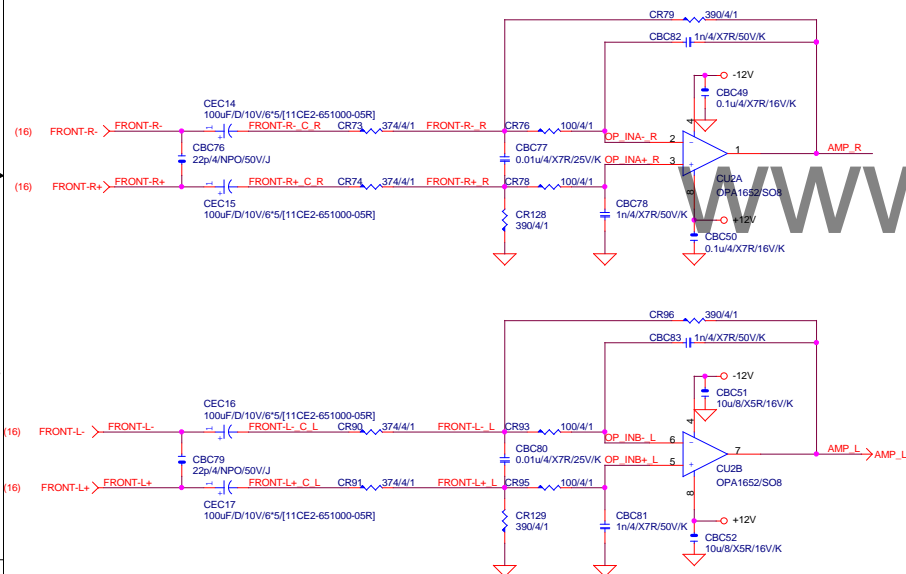


SPDIF_OUT



*量產前, 0ohm改short pad

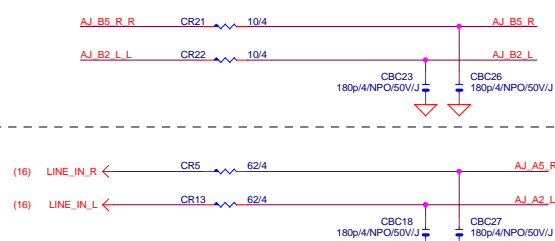
Differential to Single-End AMPLIFIED



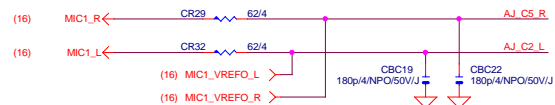
LINE-OUT

→ Audio jack -> USB(各打2 VIA hole)

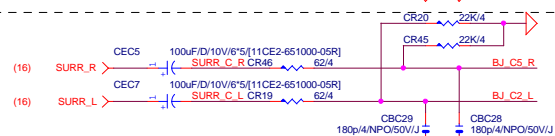
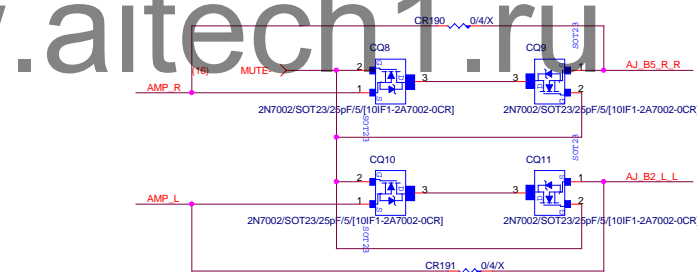
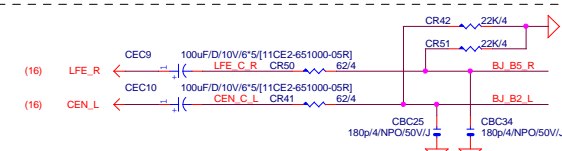
LINE-IN



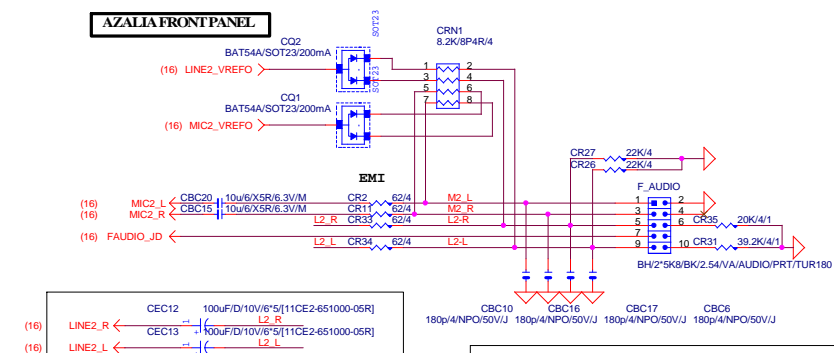
MIC-IN



SURROUND

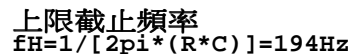
**CEN/LFE**

AZALIA FRONT PANEL

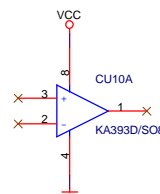
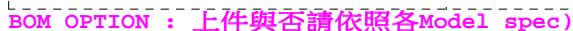


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Title				AUDIO JACK				Rev	
Size		Document Number		GA-Z170X-SOC Force				1.01	
Date: Wednesday, September 30, 2015				Sheet		17 of 88			



電壓增益
 $A_v = 1 + (R_f / R_n) = 100$ 倍




Rear Panel LED ON/OFF

ITE8620 GP83
(可以和MPD-不同步)

ITE8620 GP91

AUDIO LED Cont

	IO_GP82	IO_GP83	IO_GP91
Sill Mode	L	H	L
OFF Mode	L	L	L
Pluse Mode	L	H	BREATH
Beat Mode	OD	H	L

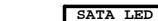
			
Title			
AUDIO LED			
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	18 of 88

TT8620E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時會拉 Lo
PIN 90/91	DEFAULT為HDLed FUNCTION GP93 BYPASS TO GP92 (2) 高溫時 GP92 會被拉Lo (ITE BUG)
PIN 108	GP40--- (POWER ON 時會拉 Lo
PIN 111/112	MOURSE 限 GAN6 FUNCTION 擇一使用,不然會互相干擾
PIN 22	PIN22, 需高於3V, 若低於搭部分COM PORT及LPT裝置蜂鳴器會異常動作。

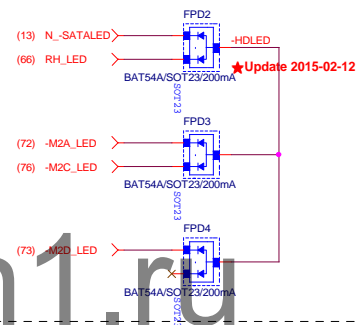
(組態二)	Intel LAN	
-------	-----------	--

JP2	1	Disable WDT
	0	Enable WDT to rest PWROK
JP3	1	SPI-Flash Disable
	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
	1 0	The default value of EC Index 63h/6Bh/73h is FFh.
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

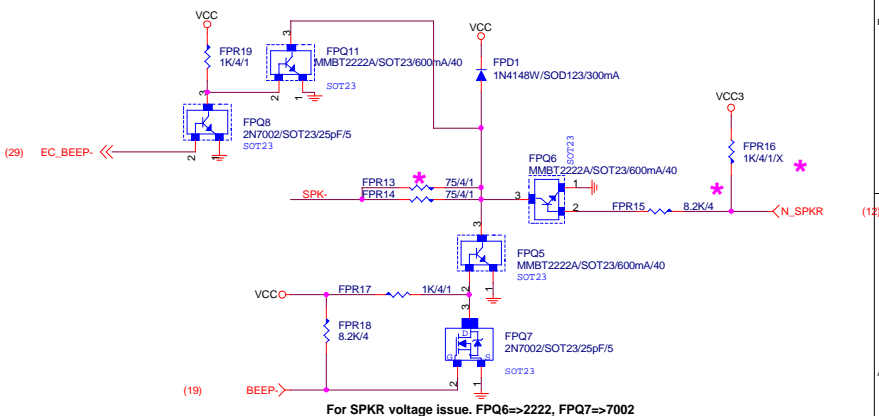
~~ERP WAKE on LAN~~



SATA LED

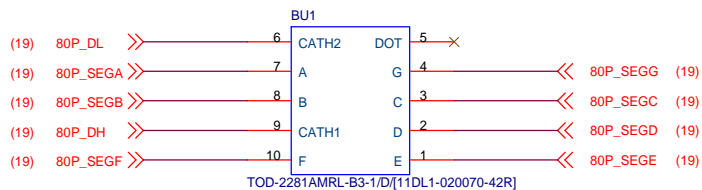
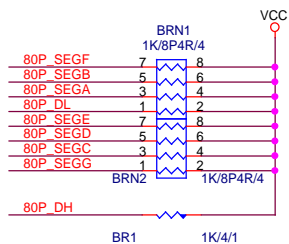


SPEAKER

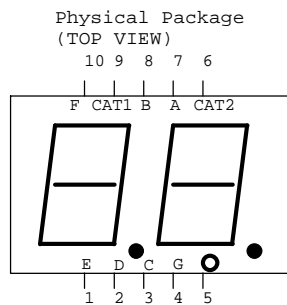


For SPKR voltage issue. FPQ6=>2222, FPQ7=>7002

80 PORT



COMMON CATHODE

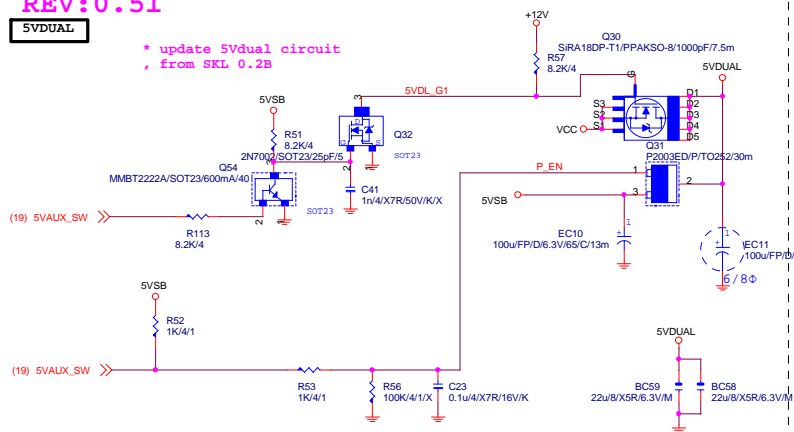


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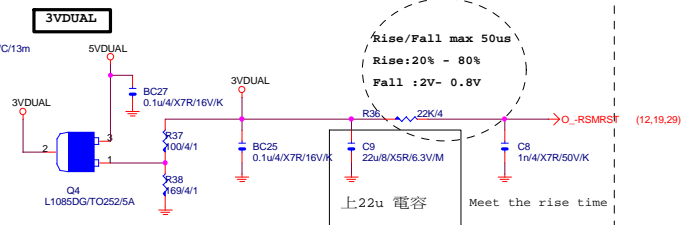
REV:0.51

5VDUAL

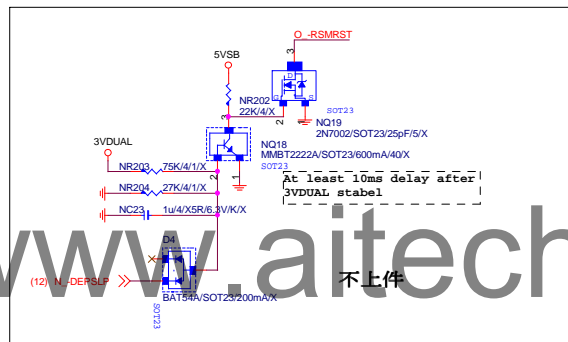
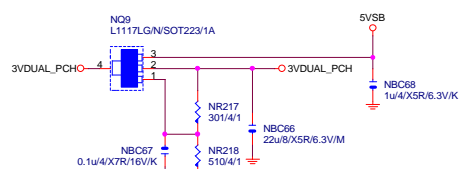
* update 5Vdual circuit
from SKL 0.2B



3VDUAL



3VDUAL_PCH

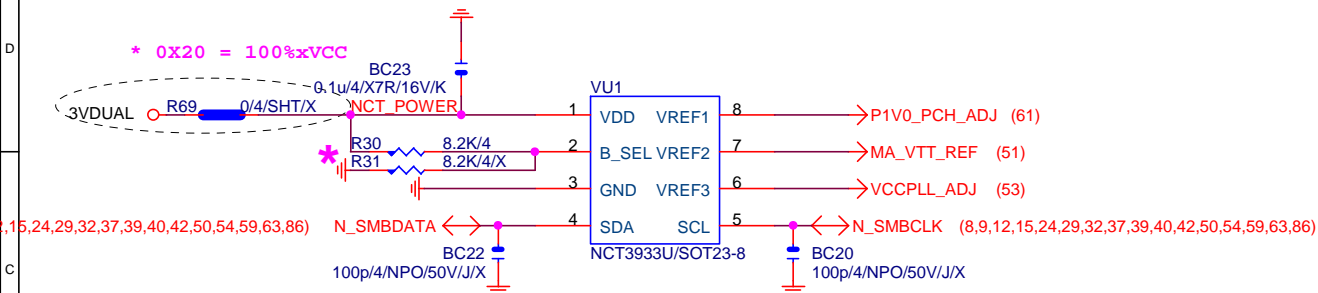


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Title		DISCRETE POWER	
Size	Document Number	GA-Z170X-SOC Force	
Custom		Rev 1.01	
Date:	Wednesday, September 30, 2015	Sheet 22	of 88

OVER VOLTAGE



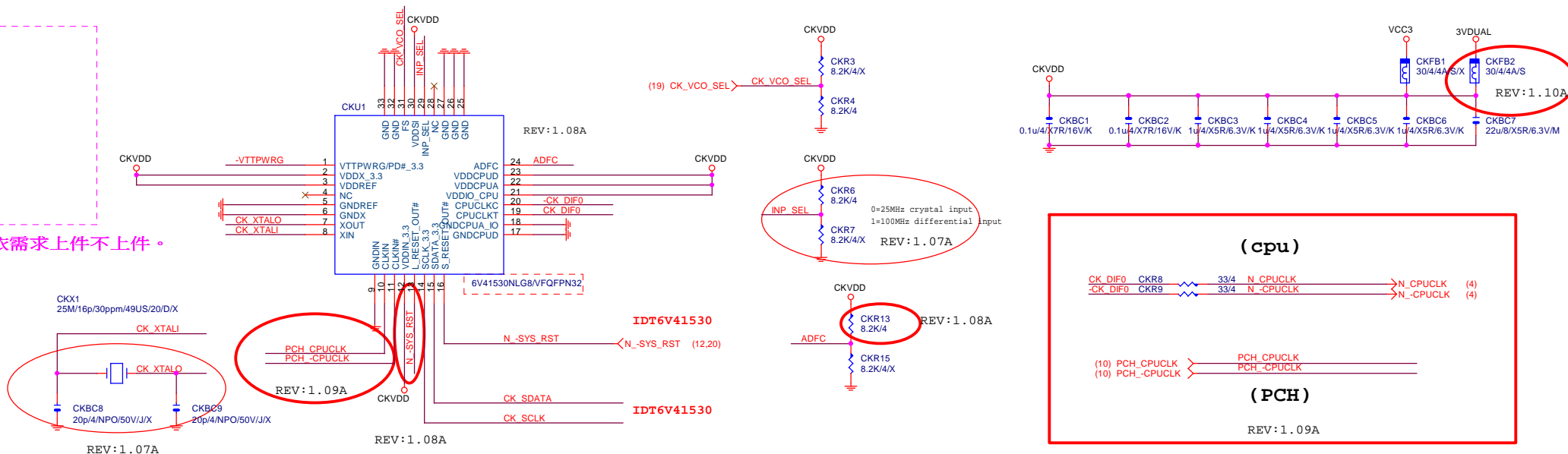
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VREF1	PCH1_0		
VREF2	MA_VTT_REF		
VREF3	N/A		

Gigabyte Technology			
NCT3933			
Title	NCT3933		
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	23 of 88

REV:1.10A

IDT6V41530

*可變, 依需求上件不上件。



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INP_SEL	Intput
0	Crystal
1	CLK_INP/N

CK_VCO_SEL	VCO
0	400M
1	1200M

GIGABYTE™			
Title			
IDT6V41530_CLK BUFFER			
Size	Document Number	Rev	
Custom	MODEL NAME	1.01	
Date:	Wednesday, September 30, 2015	Sheet	24 of 88

[illegible]

HOT MOS H/W MONITOR

RS_VCORE \ RS_VCCGT CLOSE CPU VCORE & VCCGT MOSFET
 -PROCHOT:有mos heartsink不用prochot function

(19) VREF ←

(19) TR5
 (19) TR6 ←

OC14 1u4/XSR/6.3V/K

RS_VCORE 10K/1/4/S

CLOSE VCORE MOSFET

OC15 1u4/XSR/6.3V/K

RS_VCCGT 10K/1/4/S

CLOSE VCCGT MOSFET

126~133 degree

TEMP H/W MONITOR

(19) VREF ←

(19) SYS_TEMP ←

(19) PCH_TEMP ←

(19) CPU_TEMP ←

OC7 1u4/XSR/6.3V/K

OC8 1u4/XSR/6.3V/K

OR73 10K/4/1

RS_SYS 10K/1/4/S

R675 10K/4/1

RS_PCH 10K/1/4/S

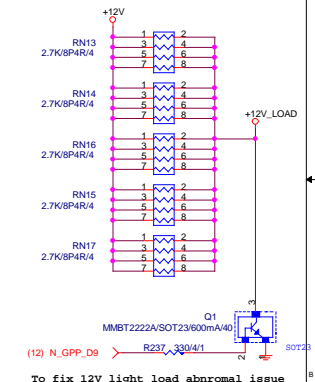
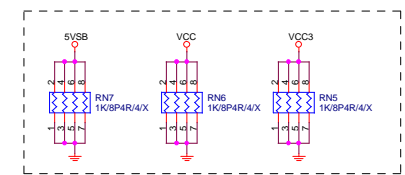
R674 10K/4/1

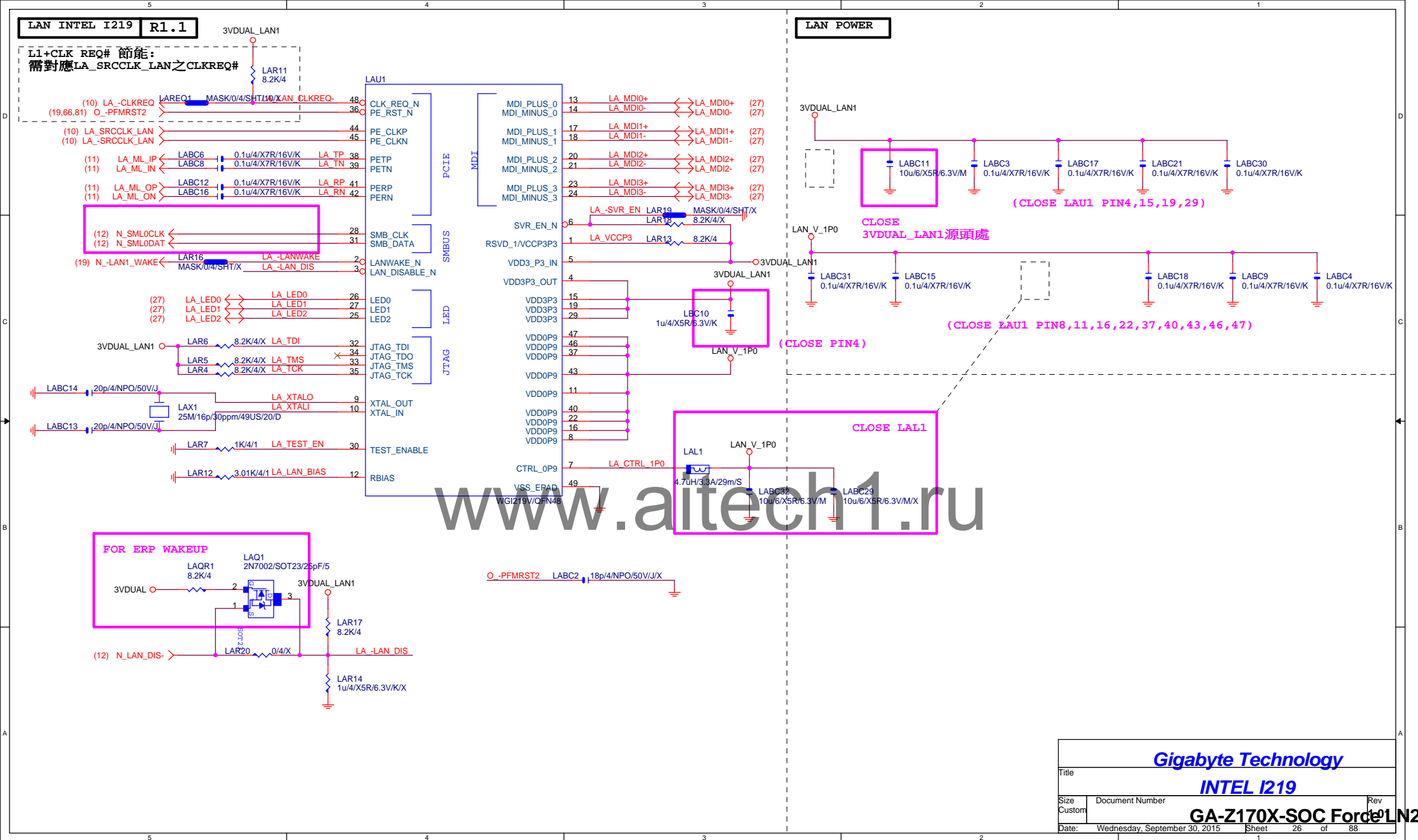
OC16 1u4/XSR/6.3V/K

TMPIN1 -

TMPIN2 -

The schematic diagram illustrates the power supply section for the CPU-Z module. It shows the connection of various power pins (VIN5, VIN6, VIN2, VIN1, VIN0) to the CPU-Z module. The diagram includes components like resistors (OR75, OR74, OR57, OR79, OR76, OR61, OC12, OR70, OC9, OC8, OC4, OC3, OR53, OR77, OC11), capacitors (OC9, OC8, OC4, OC12, OR70, OC9, OC8, OC4, OC3, OR53, OR77, OC11), and voltage regulators (VCCSA, VDDQ_SIO, VCC3, +12V, VCCGT, VCC). The diagram is labeled "for CPU-Z" and shows a 2.0V output.



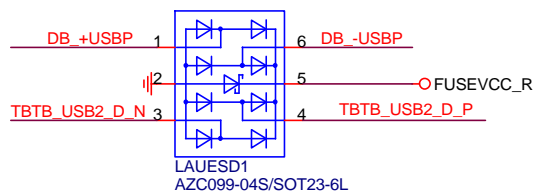


R1.09

RMA ESD PROTECT

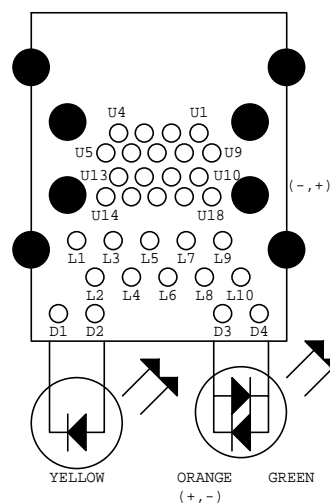
note:可變更USB NAME

可變

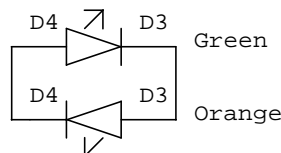


POWER 可自行調整

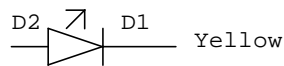
USB30_LAN LAYOUT示意圖



Dual Color LED



Single Color LED



LAN COVER

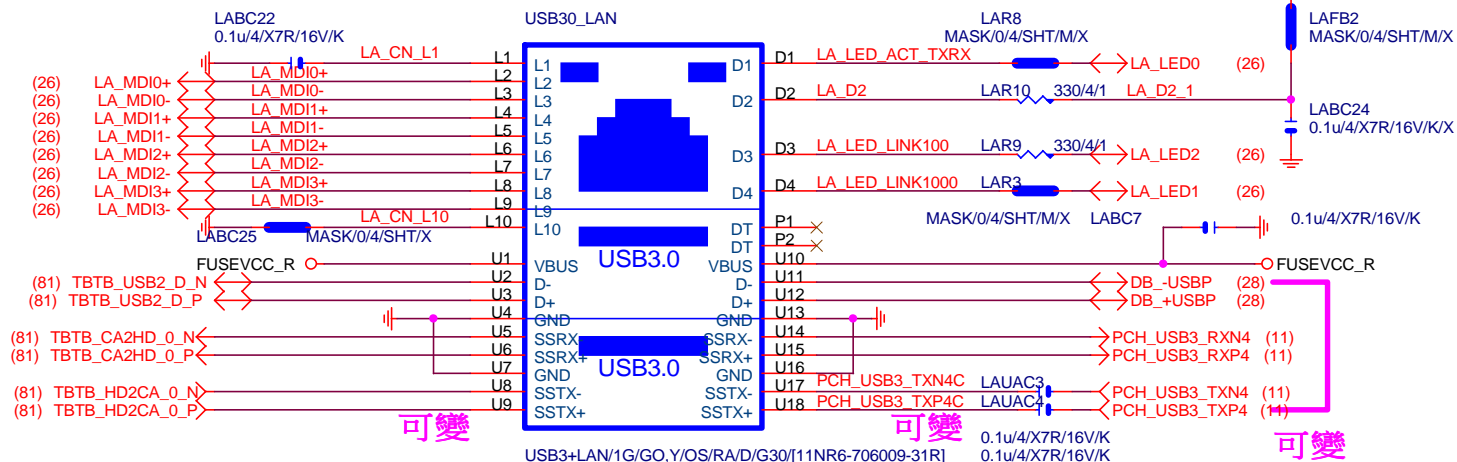
FOOT PRINT:LAN COVER

統一放在HS那頁

USB_LAN CONNECTOR

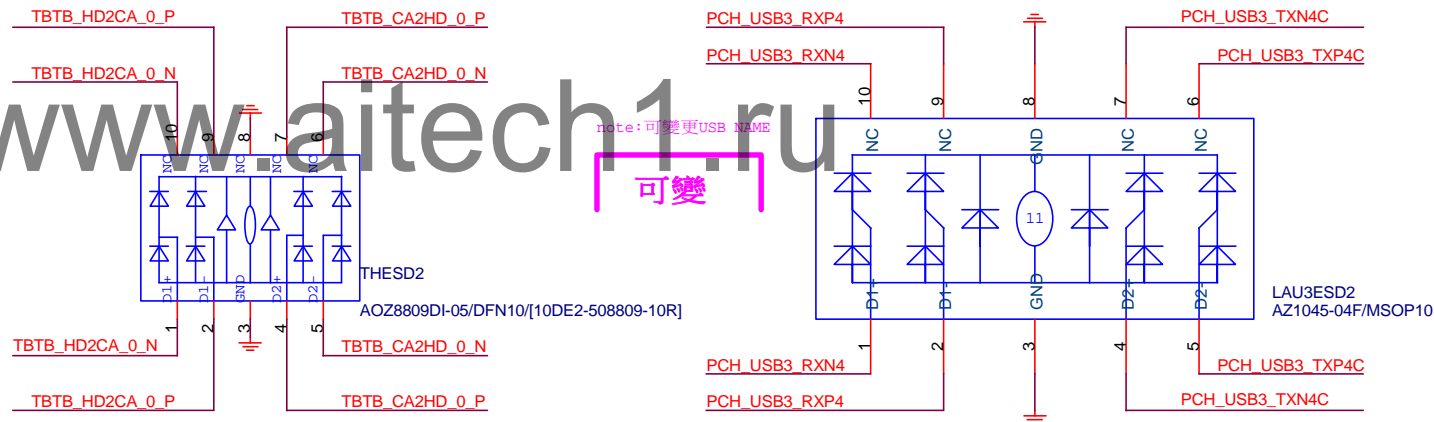
note:可變更USB NAME

[I219]



LA MDI-->100歐姆:[20/4/8/4/20]

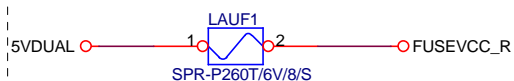
USB30_LAN LAYOUT示意圖



USB POWER

note:可變更FUSE

可變



EMI SHORT PAD

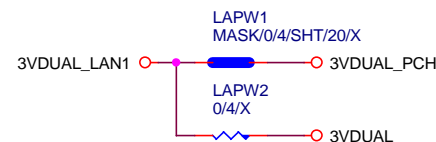
PS:視EMI需求



LAN POWER

note: lan power連接及電流

可變



Close to connector
FUSE-0805

Gigabyte Technology

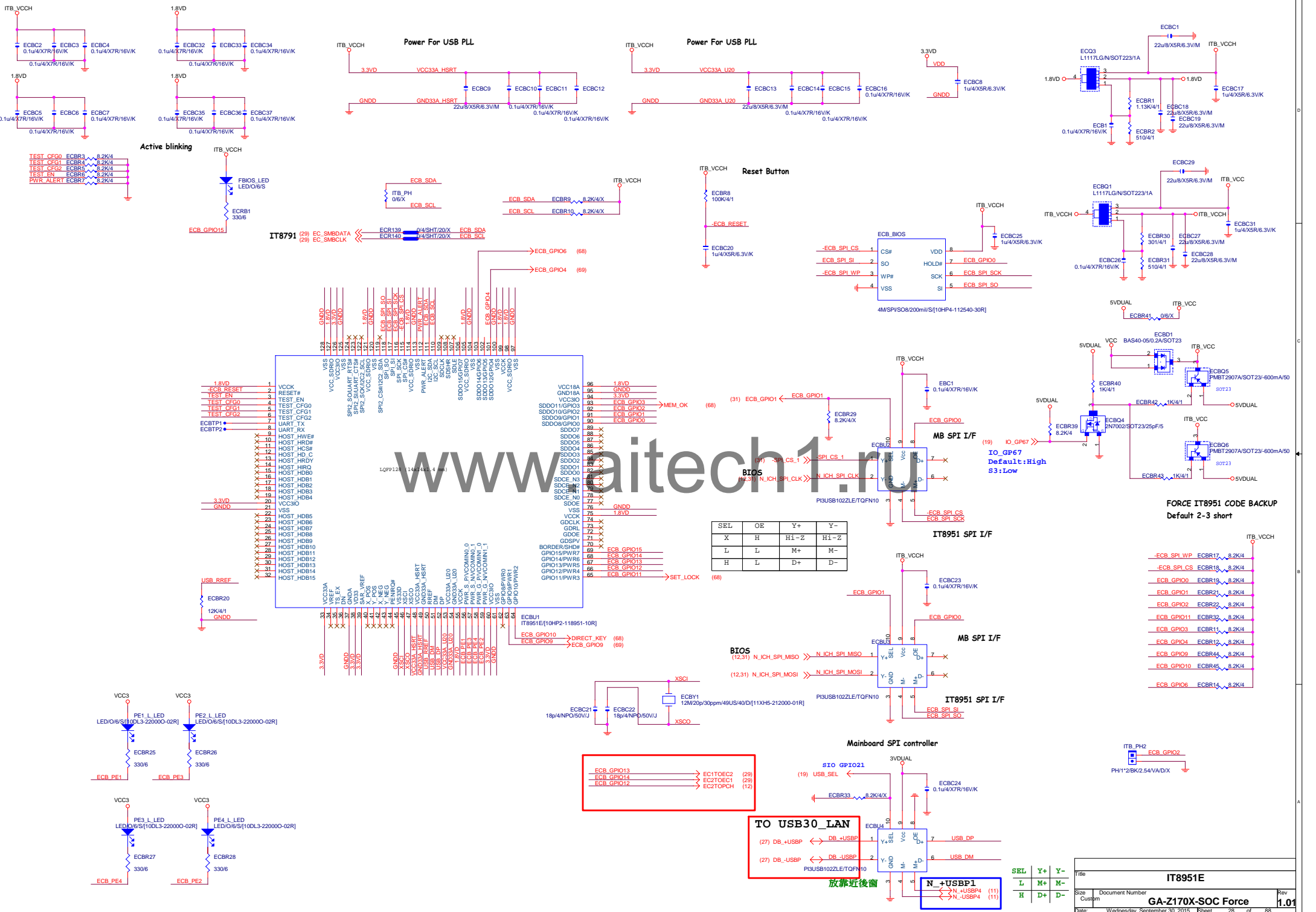
LAN CONNECTOR-I219

Size	Document Number
Custom	

GA-Z170X-SOC Force

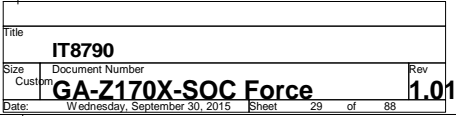
Rev

Date: Wednesday, September 30, 2015 Sheet 27 of 88



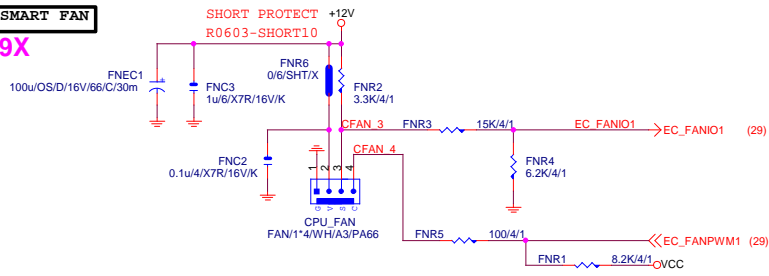
SEL	OE	Y+	Y-
X	H	H1-Z	H1-Z
L	L	M+	M-
H	L	D+	D-

IT8951E			
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	28 of 88



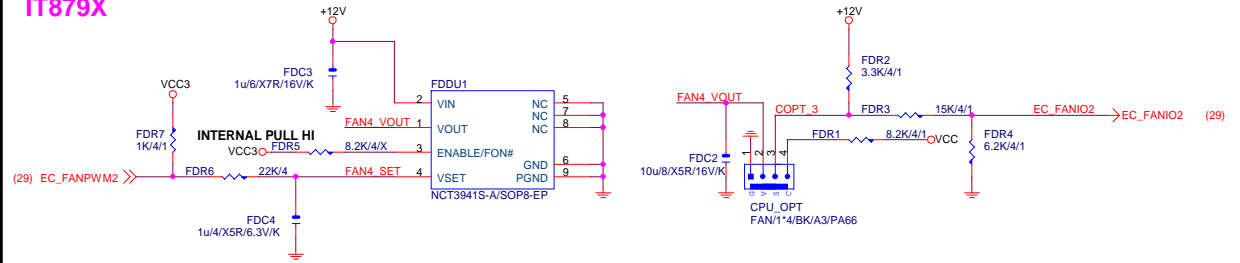
CPU SMART FAN

IT879X



CPU_OPT

IT879X

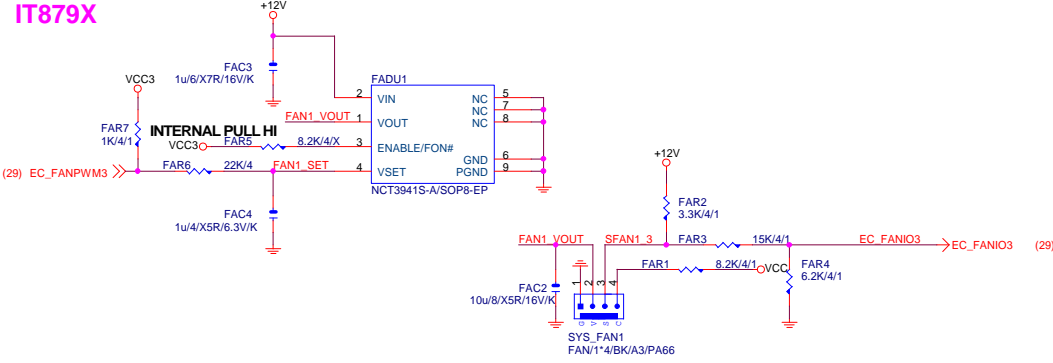


SYSTEM FAN1

IT879X

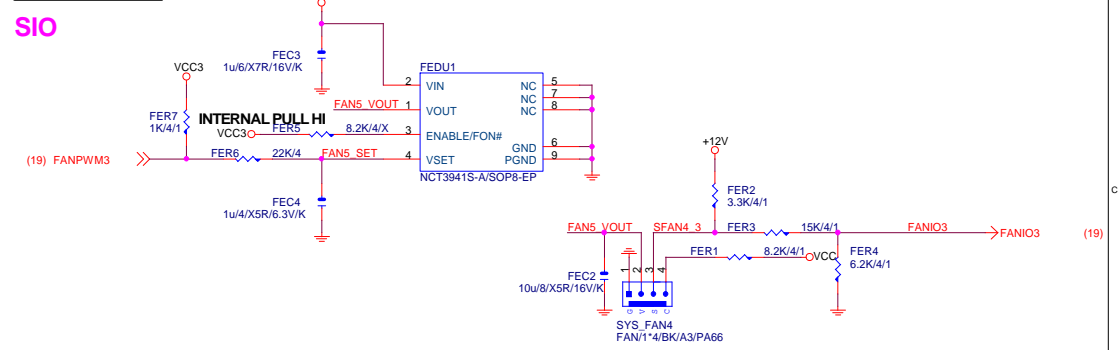
Linear SYS_FAN

Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)



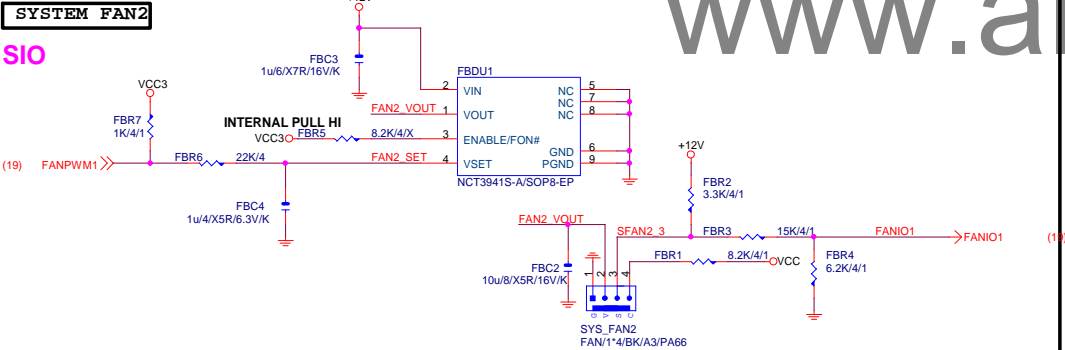
SYSTEM FAN4

SIO



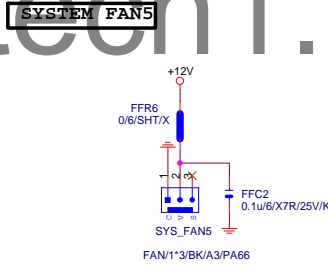
SYSTEM FAN2

SIO



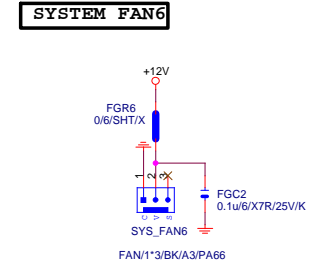
SYSTEM FAN5

SIO



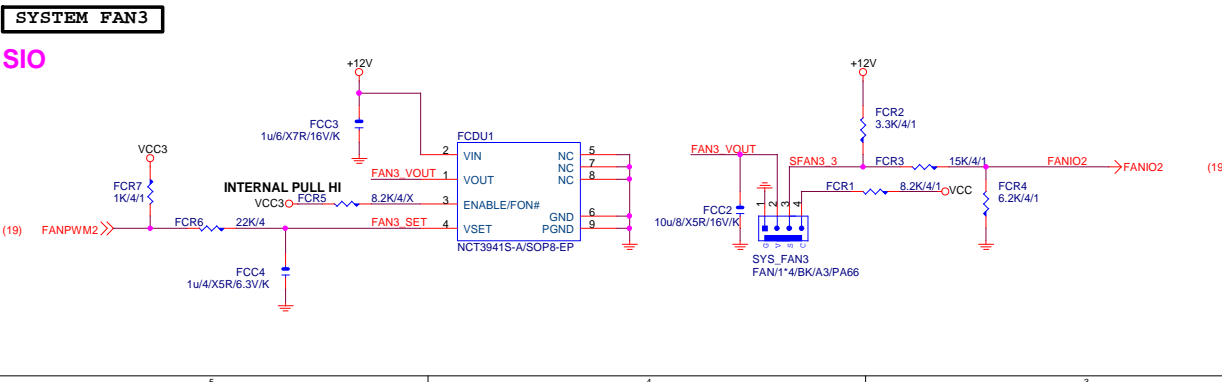
SYSTEM FAN6

SIO



SYSTEM FAN3

SIO

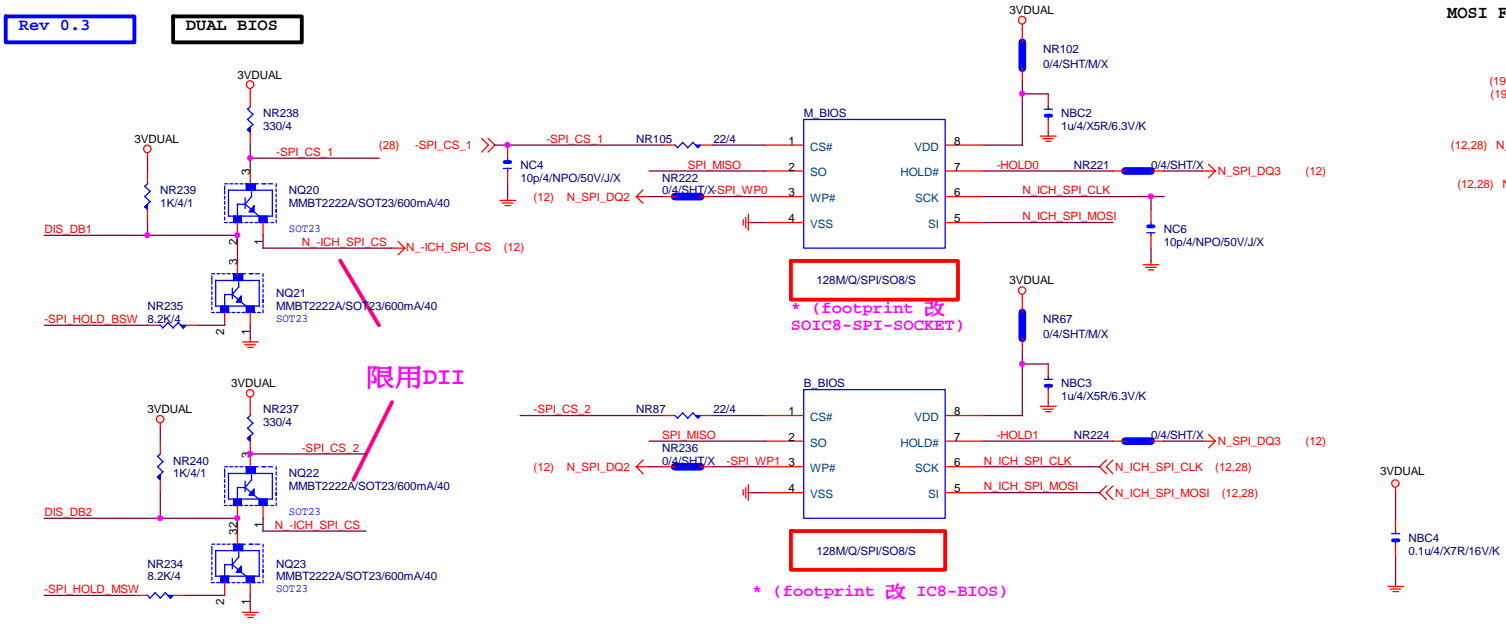


Gigabyte Technology

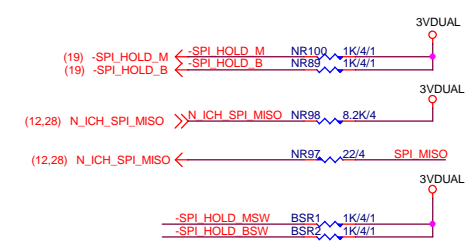
Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	30 of 88

Rev 0.3

DUAL BIOS



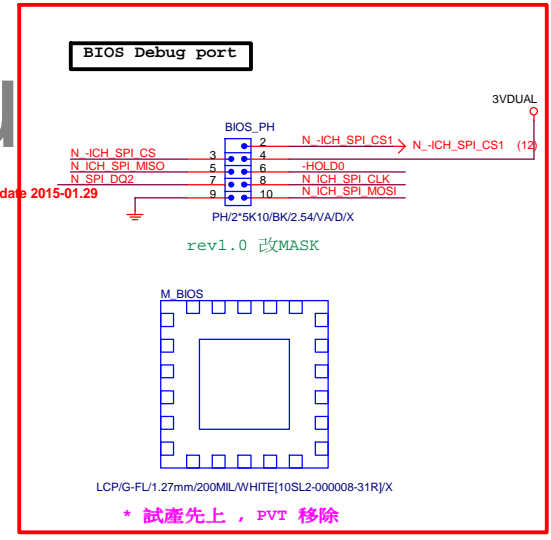
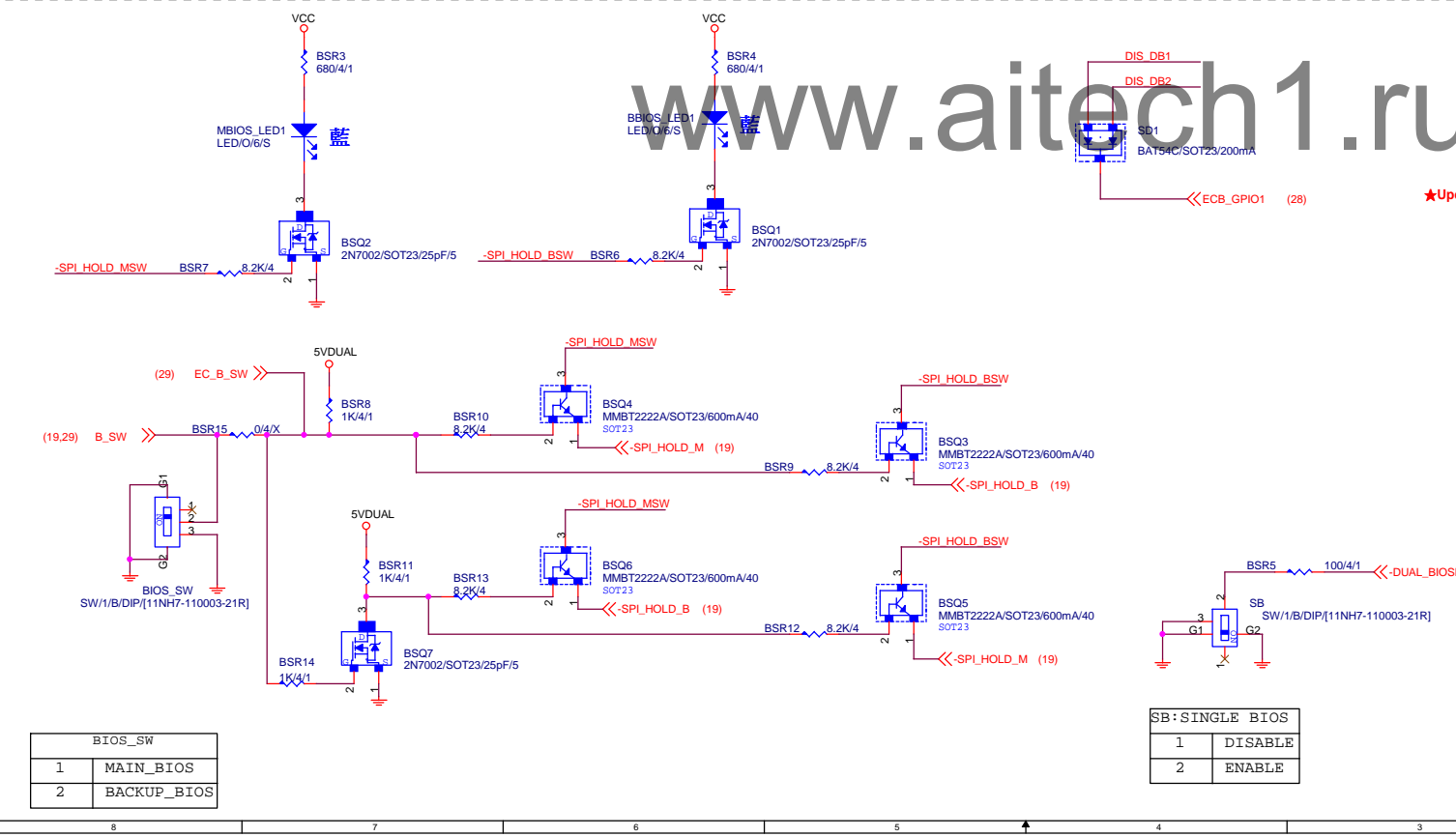
MOSI For DMI RX Termination Voltage



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

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BIOS_SW	
1	MAIN_BIOS
2	BACKUP_BIOS

SB: SINGLE BIOS	
1	DISABLE
2	ENABLE

Gigabyte Technology

Title: **Dual BIOS**

Size Custom: **GA-Z170X-SOC Force**

Date: Wednesday, September 30, 2015 Sheet 31 of 88

Rev: **1.01**

可變動

PA_EXP_TXP0_15] >>> PA_EXP_TXP0_15] (4)
PA_EXP_TXN0_15] >>> PA_EXP_TXN0_15] (4)
PA_EXP_RXP0_15] >>> PA_EXP_RXP0_15] (4)
PA_EXP_RXN0_15] >>> PA_EXP_RXN0_15] (4)

可變動
電容靠近CPU

PA_EXP_TXP15	YC169	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP15	AD1
PA_EXP_TXN15	YC170	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN15	AE1
PA_EXP_TXP14	YC171	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP14	AD2
PA_EXP_TXN14	YC172	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN14	AE2
PA_EXP_TXP13	YC173	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP13	AD4
PA_EXP_TXN13	YC174	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN13	AE4
PA_EXP_TXP12	YC175	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP12	AD5
PA_EXP_TXN12	YC176	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN12	AE5
PA_EXP_TXP11	YC177	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP11	AD7
PA_EXP_TXN11	YC178	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN11	AE7
PA_EXP_TXP10	YC179	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP10	AD8
PA_EXP_TXN10	YC180	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN10	AE8
PA_EXP_TXP9	YC181	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP9	AD10
PA_EXP_TXN9	YC182	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN9	AE10
PA_EXP_TXP8	YC183	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP8	AD11
PA_EXP_TXN8	YC184	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN8	AE11
PA_EXP_TXP7	YC185	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP7	AD13
PA_EXP_TXN7	YC186	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN7	AE13
PA_EXP_TXP6	YC187	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP6	AD14
PA_EXP_TXN6	YC188	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN6	AE14
PA_EXP_TXP5	YC189	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP5	AD16
PA_EXP_TXN5	YC190	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN5	AE16
PA_EXP_TXP4	YC191	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP4	AD17
PA_EXP_TXN4	YC192	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN4	AE17
PA_EXP_TXP3	YC193	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP3	AD18
PA_EXP_TXN3	YC194	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN3	AE18
PA_EXP_TXP2	YC195	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP2	AD20
PA_EXP_TXN2	YC196	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN2	AE20
PA_EXP_TXP1	YC197	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP1	AD22
PA_EXP_TXN1	YC198	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN1	AE22
PA_EXP_TXP0	YC199	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXP0	AD23
PA_EXP_TXN0	YC200	0.22u/4/X5R/6.3V/K	PY_EXP_A_TXN0	AE23

(10) PY_PEX_CLKP >>>
(10) -PY_PEX_CLKN >>>

1.8VCC

YR111

8.2K/4

STRAP_RESERVED0

V18

-PERST

W3

PEX_REFCLKP

JTAG_TCK

W2

PEX_REFCLKN

JTAG_TDI

V7

PEX_PERST#

JTAG_TDO

JTAG_TMS

JTAG_TRST#

STRAP_RESERVED0

NCB09

I2C_SCL0

I2C_SDA0

F7

I2C_SCL0

F2

I2C_SDA0

AD12

YR2

1K/4/1

YR1

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

I2C_SDA0

1.8VCC

YR109

8.2K/4

I2C_SCL0

YR110

8.2K/4

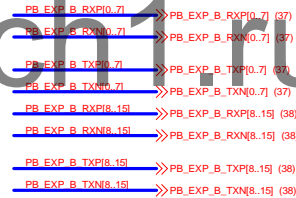
I2C_SDA0

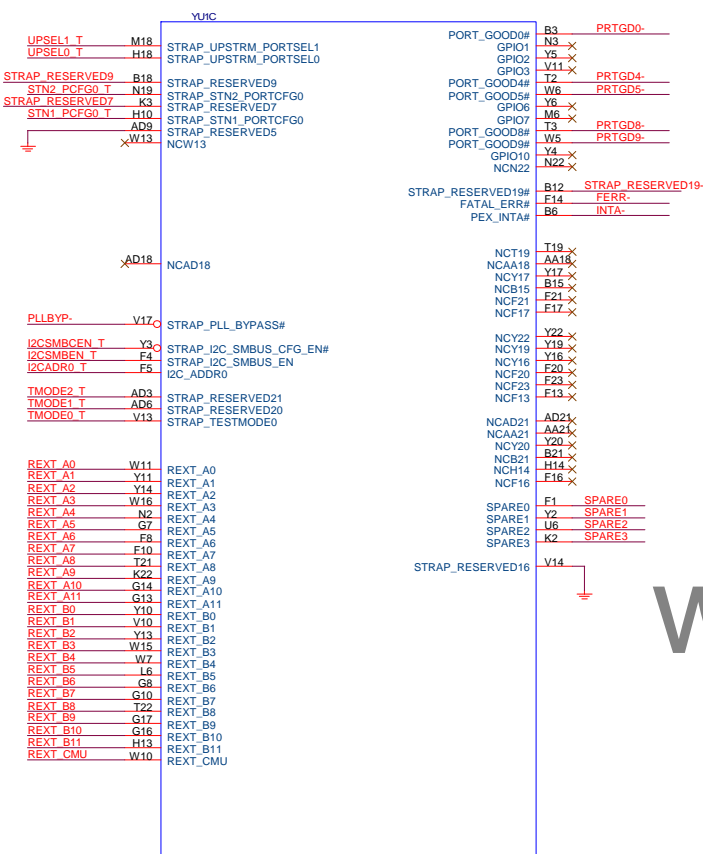
1.8VCC

YR109

8.2K/4

PA EXP A RXP0	V4	PEX_PETP16	V2	PA EXP A TXP0
PA EXP A RXN0	V5	PEX_PERN16	V1	PA EXP A TXN0
PA EXP A RXP1	U4	PEX_PETP17	U2	PA EXP A TXP1
PA EXP A RXN1	U5	PEX_PETP18	U1	PA EXP A TXN1
PA EXP A RXP2	R5	PEX_PETP19	R2	PA EXP A TXP2
PA EXP A RXN2	R4	PEX_PETP20	R1	PA EXP A TXN2
PA EXP A RXP3	P5	PEX_PETP21	P2	PA EXP A TXP3
PA EXP A RXN3	P4	PEX_PETP22	P1	PA EXP A TXN3
PA EXP A RXP4	M5	PEX_PETP23	M2	PA EXP A TXP4
PA EXP A RXN4	M4	PEX_PETP24	M1	PA EXP A TXN4
PA EXP A RXP5	L5	PEX_PETP25	L2	PA EXP A TXP5
PA EXP A RXN5	L4	PEX_PETP26	L1	PA EXP A TXN5
PA EXP A RXP6	J5	PEX_PETP27	J2	PA EXP A TXP6
PA EXP A RXN6	J4	PEX_PETP28	J1	PA EXP A TXN6
PA EXP A RXP7	H5	PEX_PETP29	H2	PA EXP A TXP7
PA EXP A RXN7	H4	PEX_PETP30	H1	PA EXP A TXN7
PA EXP A RXP8	E5	PEX_PETP31	E2	PA EXP A TXP8
PA EXP A RXN8	E4	PEX_PETP32	E1	PA EXP A TXN8
PA EXP A RXP9	D5	PEX_PETP33	D2	PA EXP A TXP9
PA EXP A RXN9	D4	PEX_PETP34	D1	PA EXP A TXN9
PA EXP A RXP10	C5	PEX_PETP35	C2	PA EXP A TXP10
PA EXP A RXN10	C4	PEX_PETP36	C1	PA EXP A TXN10
PA EXP A RXP11	B5	PEX_PETP37	B2	PA EXP A TXP11
PA EXP A RXN11	B4	PEX_PETP38	B1	PA EXP A TXN11
PA EXP A RXP12	A5	PEX_PETP39	A2	PA EXP A TXP12
PA EXP A RXN12	A4	PEX_PETP40	A1	PA EXP A TXN12
PA EXP A RXP13	D7	PEX_PETP41	D2	PA EXP A TXP13
PA EXP A RXN13	D6	PEX_PETP42	D1	PA EXP A TXN13
PA EXP A RXP14	E10	PEX_PETP43	E2	PA EXP A TXP14
PA EXP A RXN14	E9	PEX_PETP44	E1	PA EXP A TXN14
PA EXP A RXP15	F11	PEX_PETP45	F2	PA EXP A TXP15
PA EXP A RXN15	F10	PEX_PETP46	F1	PA EXP A TXN15
PB EXP B RXP0	V19	PEX_PETP47	V22	PB EXP B TXP0
PB EXP B RXN0	V20	PEX_PETP48	V23	PB EXP B TXN0
PB EXP B RXP1	U19	PEX_PETP49	U22	PB EXP B TXP1
PB EXP B RXN1	U20	PEX_PETP50	U23	PB EXP B TXN1
PB EXP B RXP2	R19	PEX_PETP51	R22	PB EXP B TXP2
PB EXP B RXN2	R20	PEX_PETP52	R23	PB EXP B TXN2
PB EXP B RXP3	P19	PEX_PETP53	P22	PB EXP B TXP3
PB EXP B RXN3	P20	PEX_PETP54	P23	PB EXP B TXN3
PB EXP B RXP4	M19	PEX_PETP55	M22	PB EXP B TXP4
PB EXP B RXN4	M20	PEX_PETP56	M23	PB EXP B TXN4
PB EXP B RXP5	L19	PEX_PETP57	L22	PB EXP B TXP5
PB EXP B RXN5	L20	PEX_PETP58	L23	PB EXP B TXN5
PB EXP B RXP6	J19	PEX_PETP59	J22	PB EXP B TXP6
PB EXP B RXN6	J20	PEX_PETP60	J23	PB EXP B TXN6
PB EXP B RXP7	H19	PEX_PETP61	H22	PB EXP B TXP7
PB EXP B RXN7	H20	PEX_PETP62	H23	PB EXP B TXN7
PB EXP B RXP8	E23	PEX_PETP63	E22	PB EXP B TXP8
PB EXP B RXN8	E22	PEX_PETP64	E23	PB EXP B TXN8
PB EXP B RXP9	D23	PEX_PETP65	D22	PB EXP B TXP9
PB EXP B RXN9	D22	PEX_PETP66	D23	PB EXP B TXN9
PB EXP B RXP10	C20	PEX_PETP67	C22	PB EXP B TXP10
PB EXP B RXN10	C20	PEX_PETP68	C23	PB EXP B TXN10
PB EXP B RXP11	E19	PEX_PETP69	E22	PB EXP B TXP11
PB EXP B RXN11	D19	PEX_PETP70	D22	PB EXP B TXN11
PB EXP B RXP12	E17	PEX_PETP71	E23	PB EXP B TXP12
PB EXP B RXN12	D17	PEX_PETP72	D23	PB EXP B TXN12
PB EXP B RXP13	E16	PEX_PETP73	E22	PB EXP B TXP13
PB EXP B RXN13	D16	PEX_PETP74	D22	PB EXP B TXN13
PB EXP B RXP14	E14	PEX_PETP75	E23	PB EXP B TXP14
PB EXP B RXN14	D14	PEX_PETP76	D23	PB EXP B TXN14
PB EXP B RXP15	E13	PEX_PETP77	E22	PB EXP B TXP15
PB EXP B RXN15	D13	PEX_PETP78	D22	PB EXP B TXN15



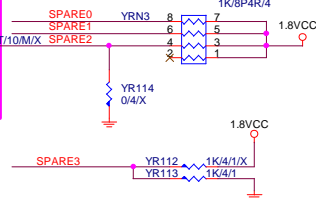


PEX8747BA80FBCGBGA575(10TA10887420R)

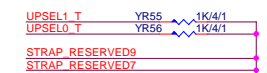
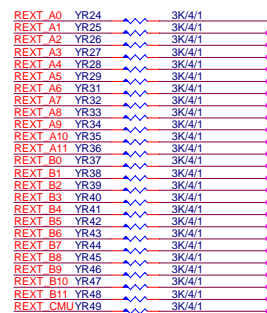
可變動

(19) IO_GP27 ← YR115 0/4/SH7/10M/X SPARE2

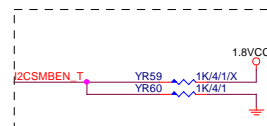
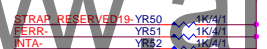
from Open-Drain standby GPIO
(default : Hi)
(Lo : GenI compatibility)



Resistors should be placed close to YU1



PLLBY-

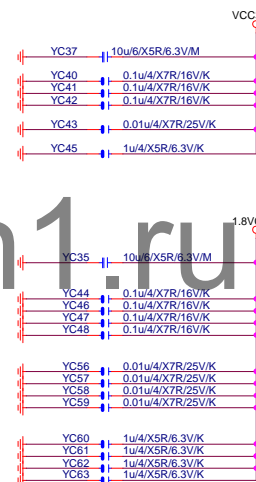
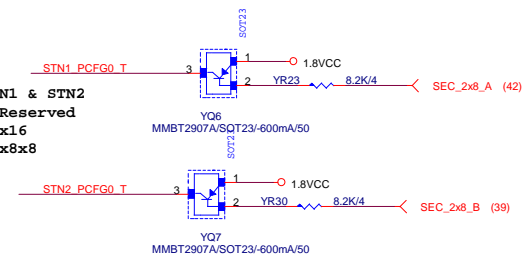


STRAP STN1 & STN2

0 = 0 = Reserved

Z = 1 = x16

1 = 2 = x8x8



1.8V_D

0.9V_A

0.9V_D

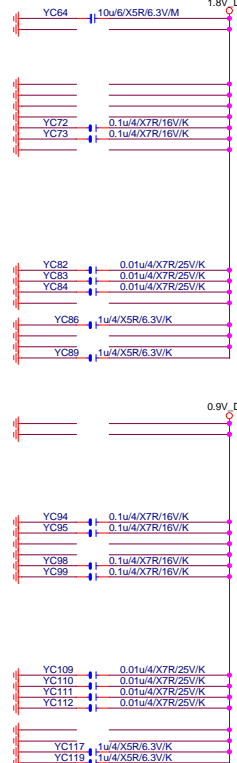
YUHE



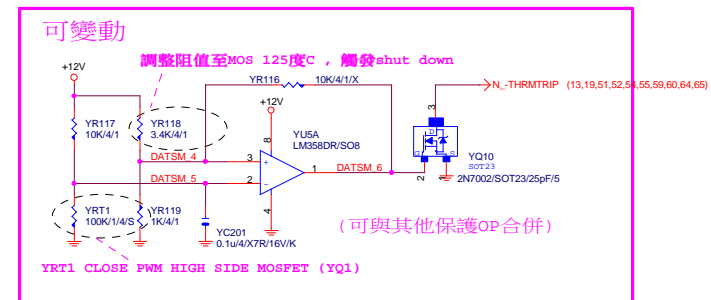
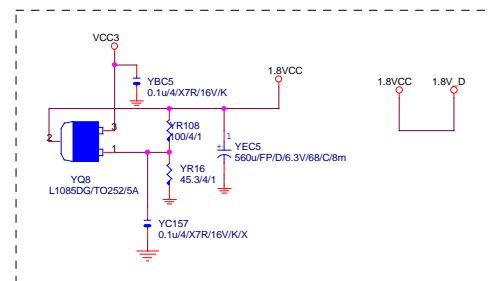
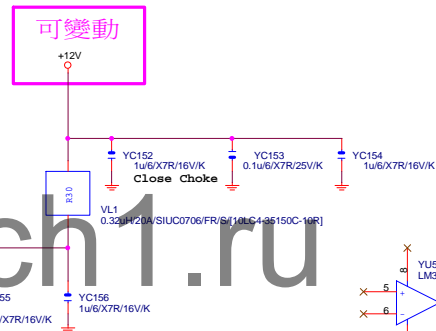
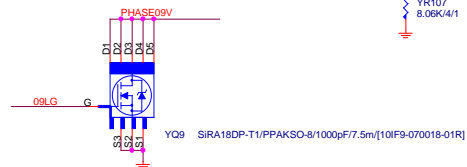
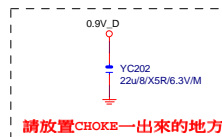
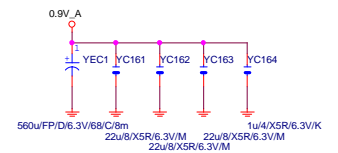
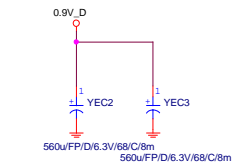
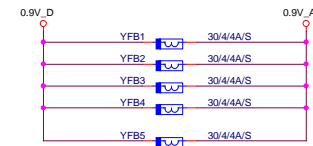
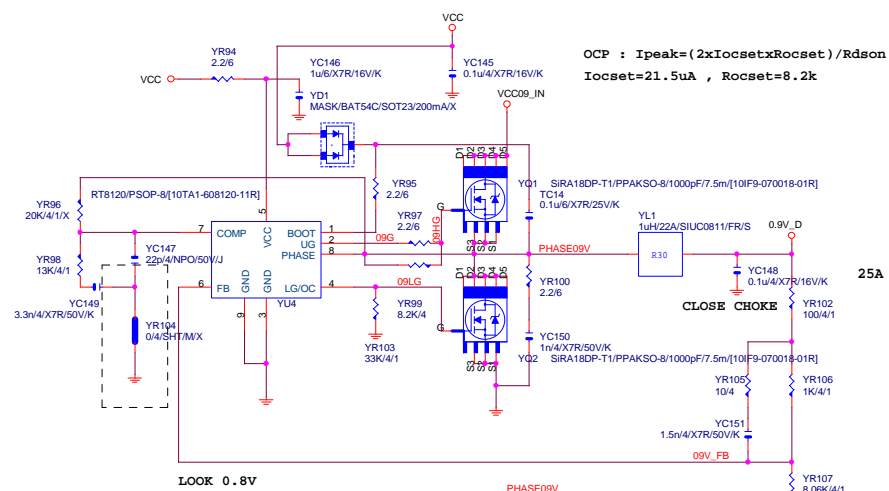
PEX8747SAB0FBCBGGA75[10TA1-088747-20R]

1.8V_D

0.9V_D

**GIGABYTE™**

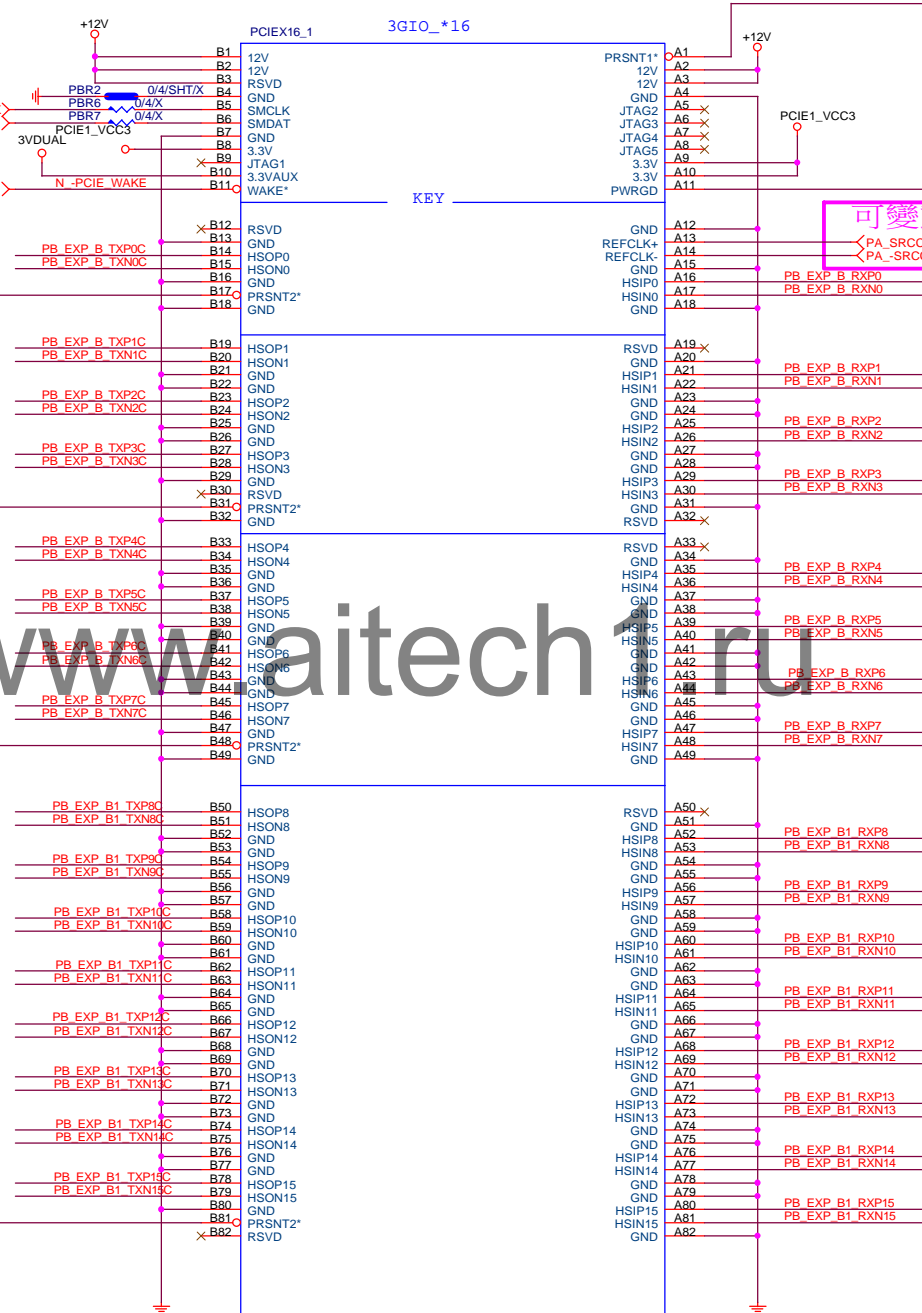
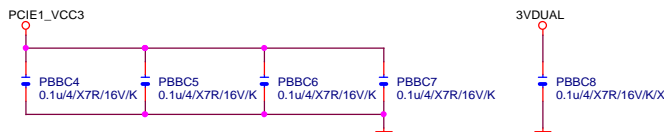
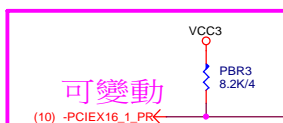
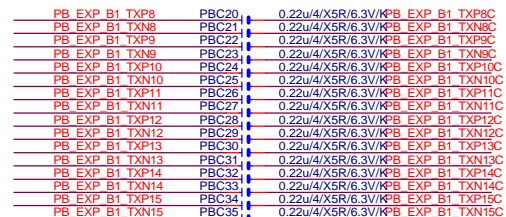
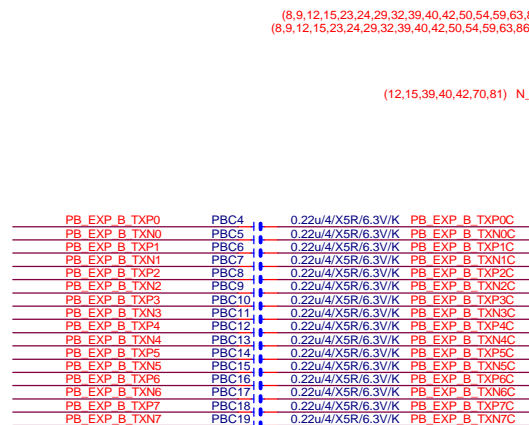
Title				
PEX8747S POWER				
Size	Document Number			Rev
Custom	GA-Z170X-SOC Force			1.01
Date:	Wednesday, September 30, 2015	Sheet	35 of	88

**GIGABYTE™**

Title		
PEX8747 POWER DESIGN		
Size	Document Number	Rev
Custom	GA-Z170X-SOC Force	1.01
Date:	Wednesday, September 30, 2015	Sheet 36 of 88



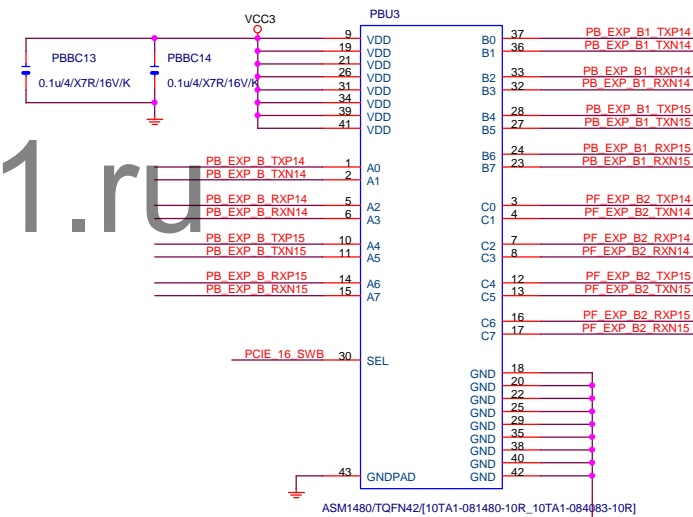
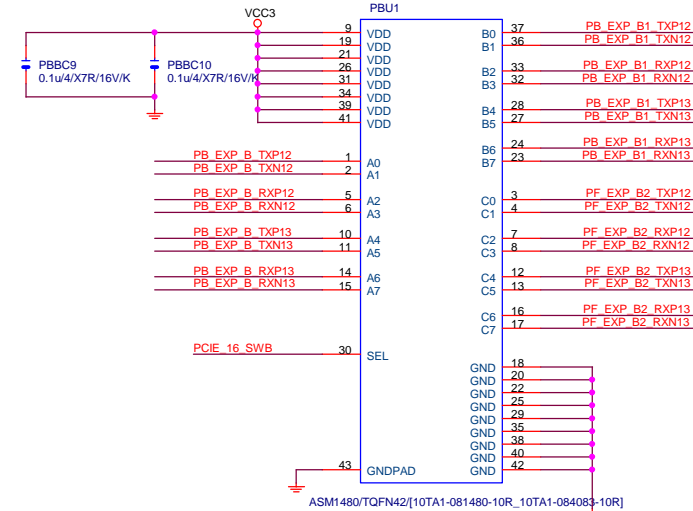
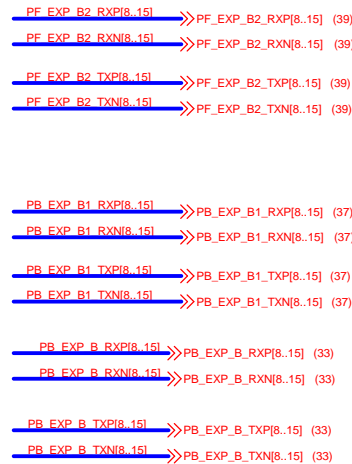
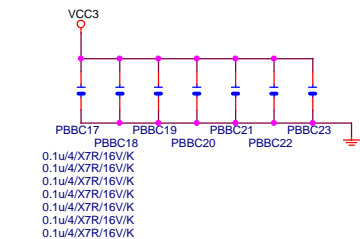
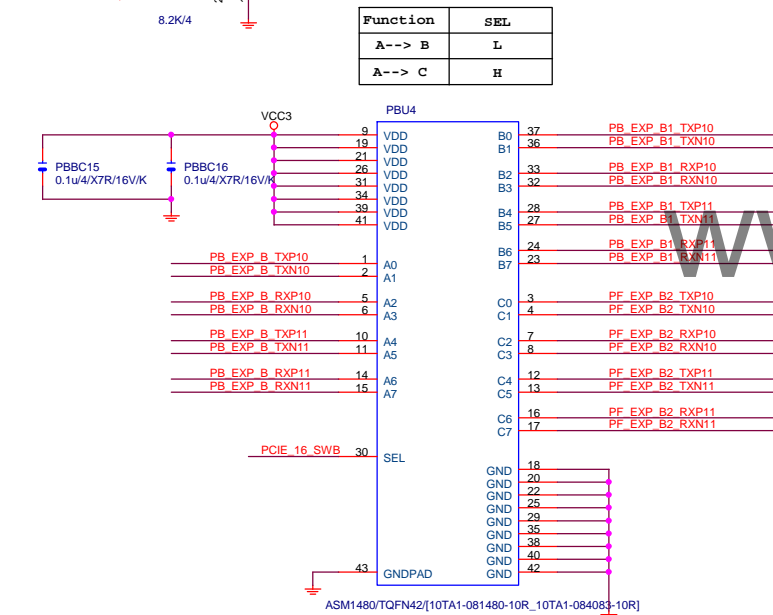
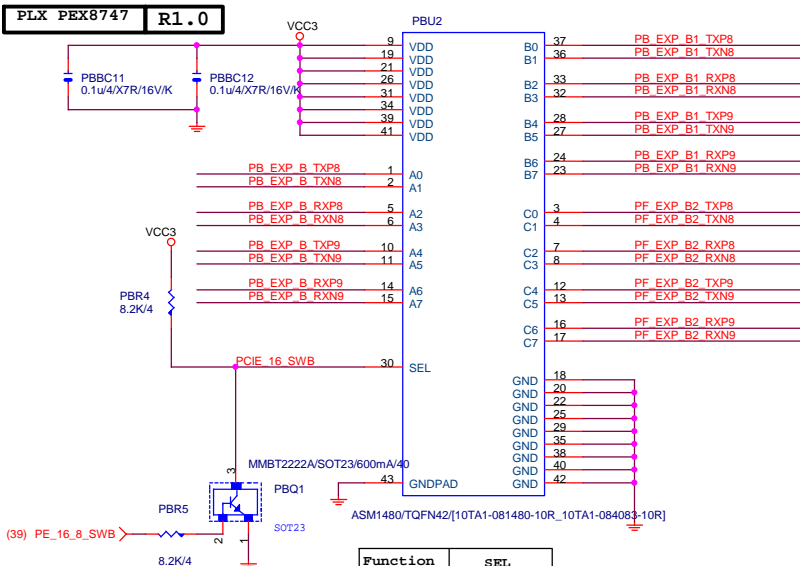
PCIESLOT-164DN-2

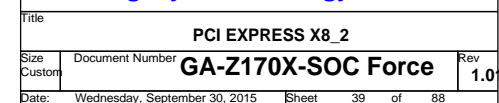


PCI-E/16X-164P/OR/GF/LONG DOUBLE/METEL HK/[11AC1-023164-F1R



Title			
PCI EXPRESS X16 PORT_2			
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet 37 of 88	



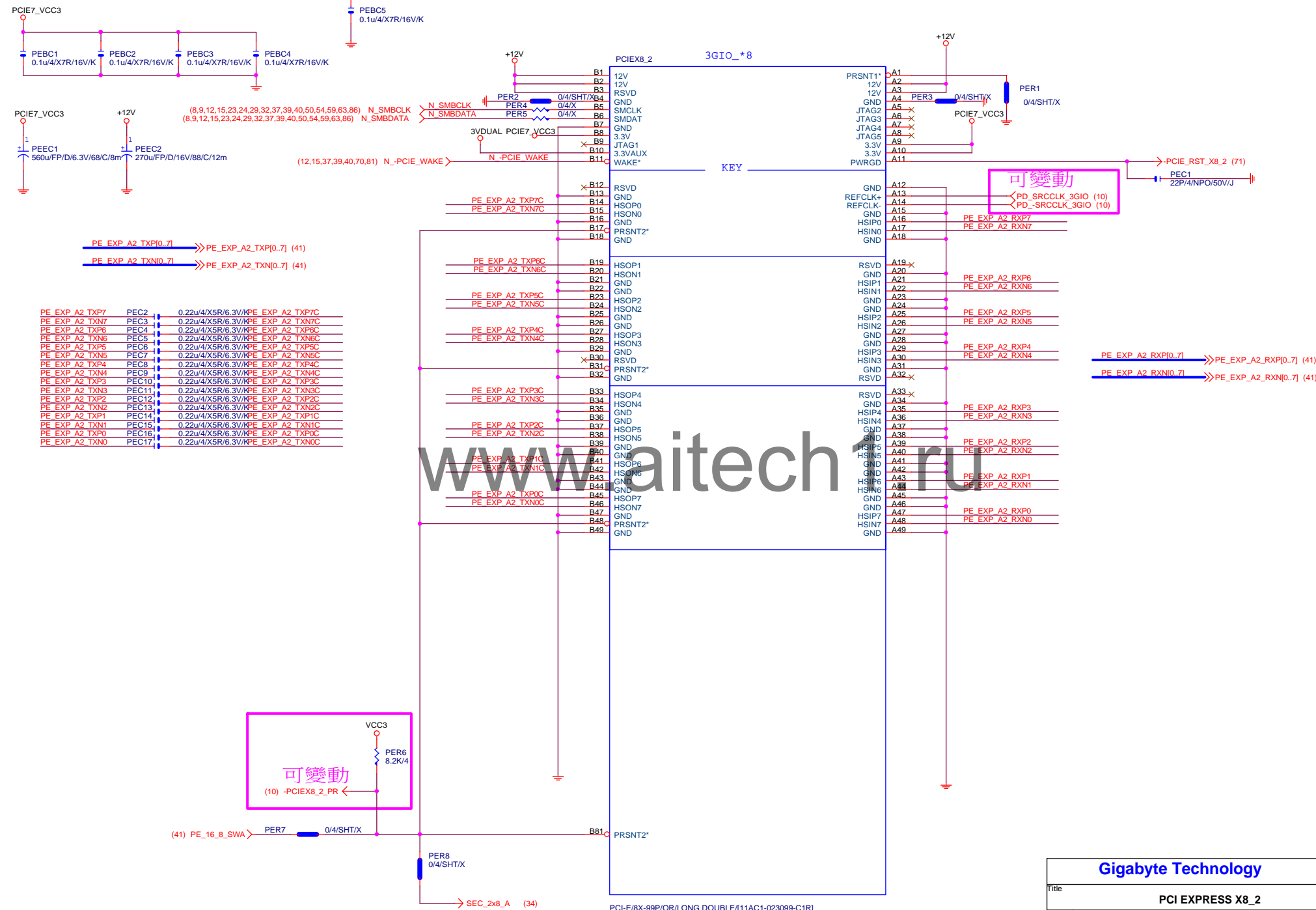


PCIESLOT-164DN-2

**GIGABYTE™**

Title	PCI EXPRESS X16 PORT_1
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Size Custom	Document Number GA-Z170X-SOC Force	Rev 1.01
Date: Wednesday, September 30, 2015	Sheet 40 of 88	



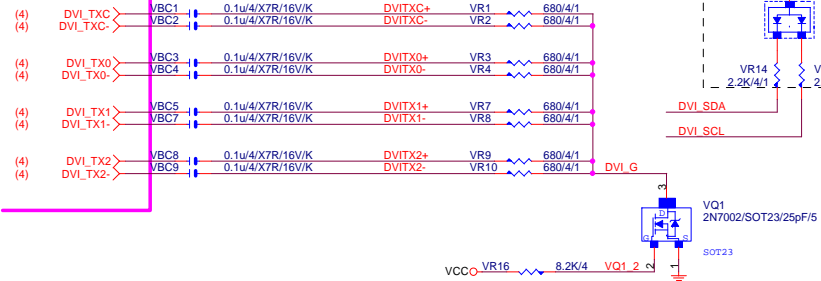
Gigabyte Technology

Title			
PCI EXPRESS X8_2			
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	42 of 88

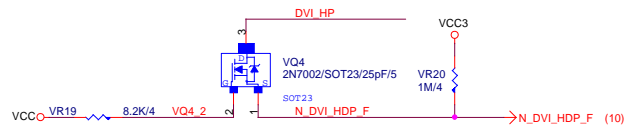
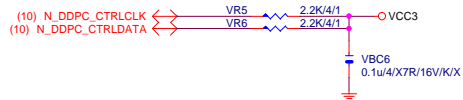
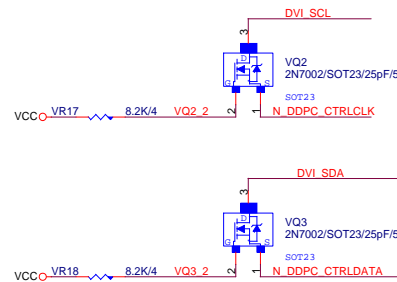
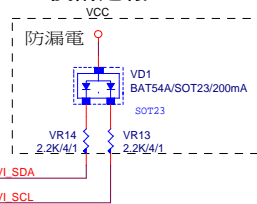
DVI CONN

DVI:20/4/6/4/20
Impedance=85 +- 17.5%

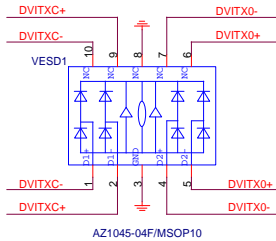
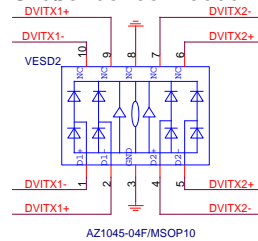
NET 可變



R&D技術通報 162

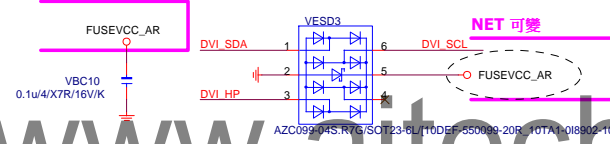


Close to connector

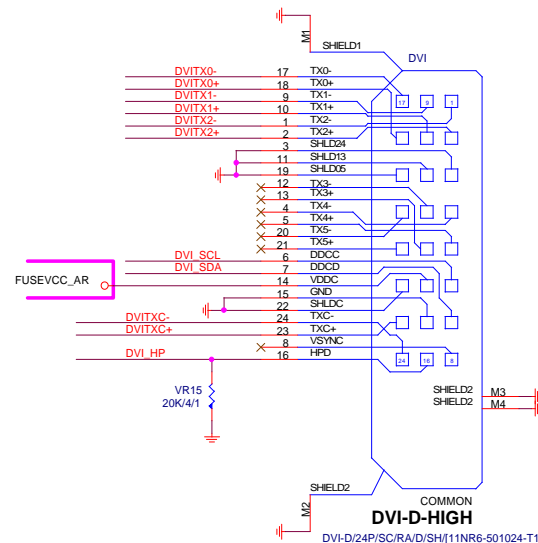
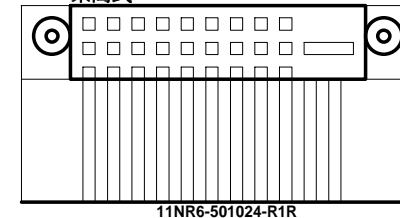


NET 可變

Close to connector



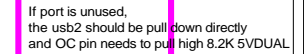
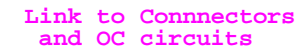
架高式 DVI-D



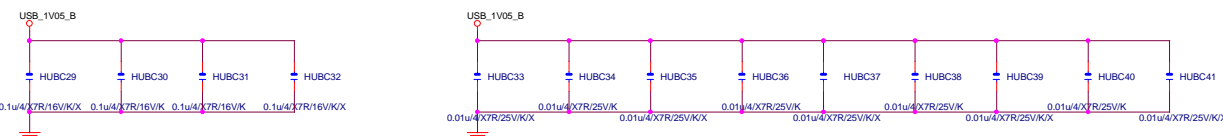
GIGABYTE

Title		DVI
Document Number		GA-Z170X-SOC For
Size	Custom	Rev 1.01
Date:	Wednesday, September 30, 2015	Sheet 43 of 88



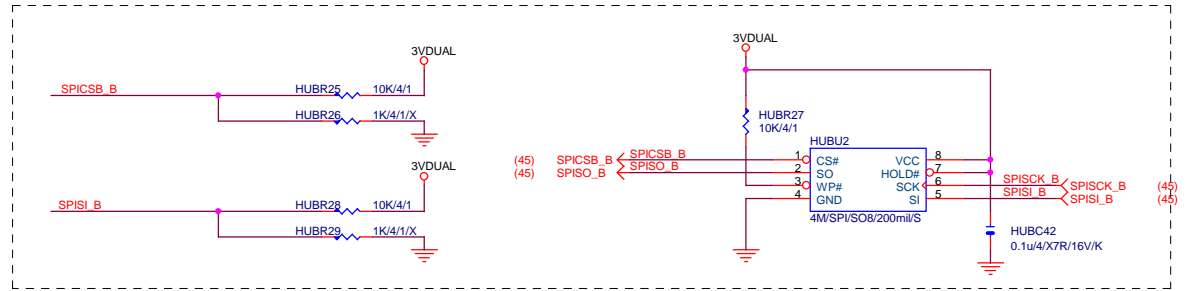


If port is unused,
the usb2 should be pull down directly
and OC pin needs to pull high 8.2K 5VDUAL

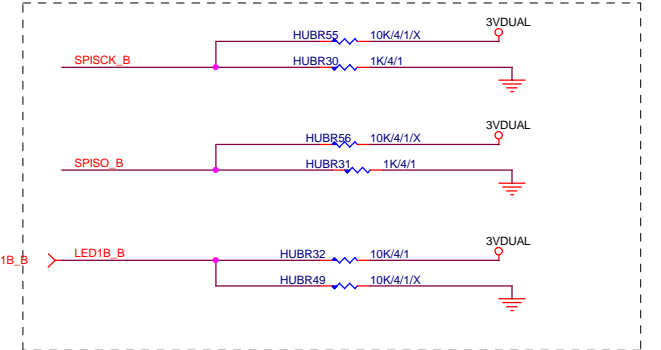


Dual USB3 HUB used

External SPI ROM ; SPI ROM attached mode

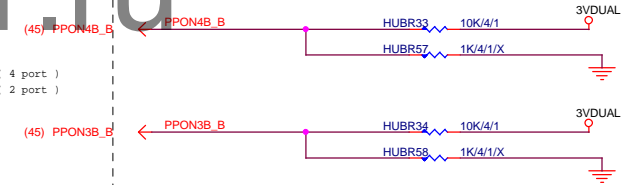


Battery Charging

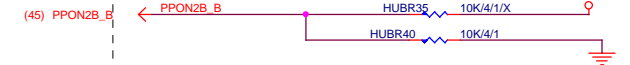


Number of Ports ; 4Ports mode

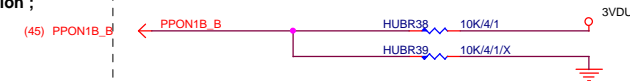
PPON3B / PPON4B : H / H (4 port)
PPON3B / PPON4B : L / L (2 port)



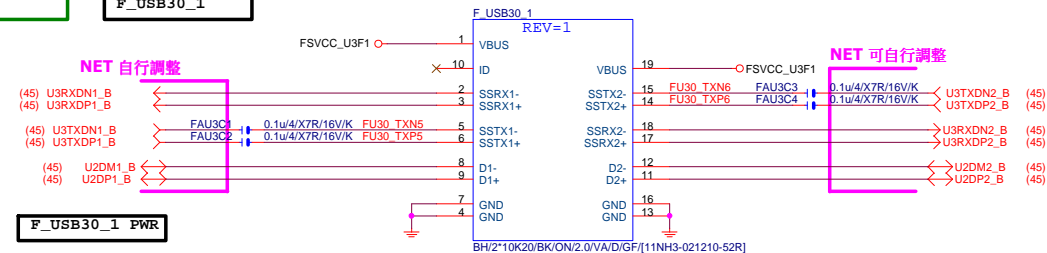
#5 VBUS Power Control ; Individual mode



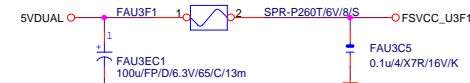
PPON1B Pin Function ; Port1 PPONB mode



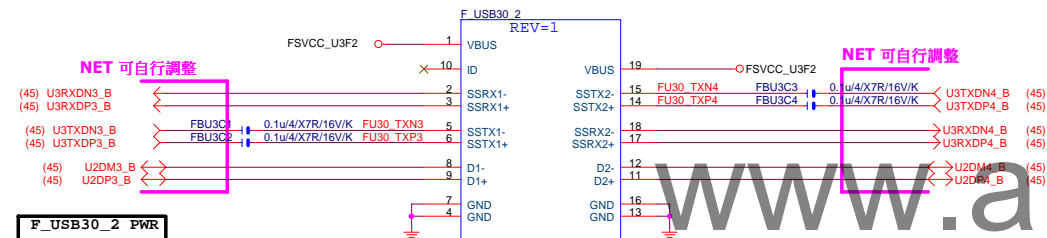
F_USB30_1



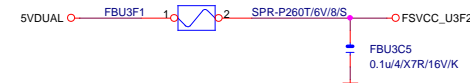
F_USB30_1	PWR
-----------	-----



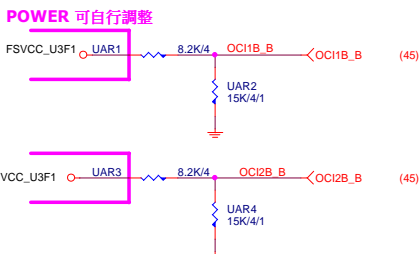
F_USB30_2



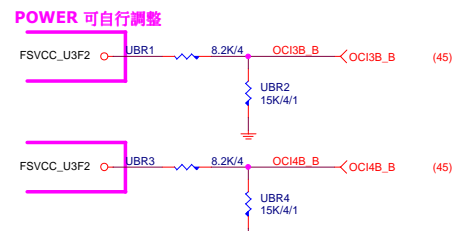
F_USB30_2 PWR



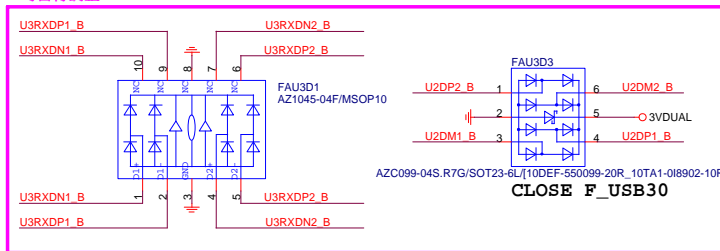
F_USB30_1



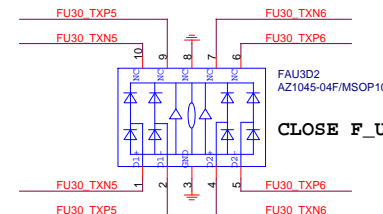
F_USB30_2



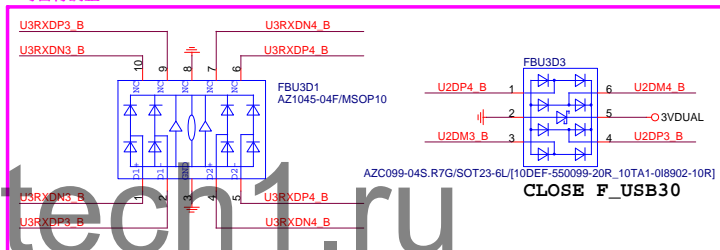
NET 可自行調整



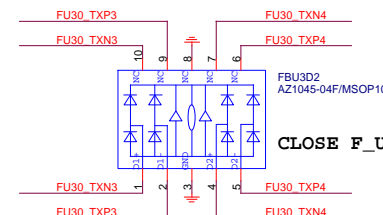
CLOSE F_USB30



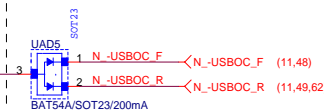
NET 可自行調整



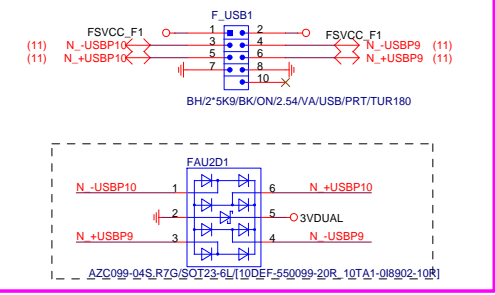
CLOSE F USB30



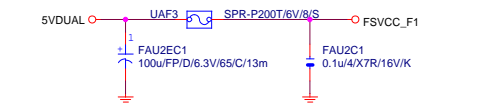
```
* 接 PCH
N_GPP_B20(SMI)
PCH PU 3Vdual
(12) N_GPP_B20 <
```



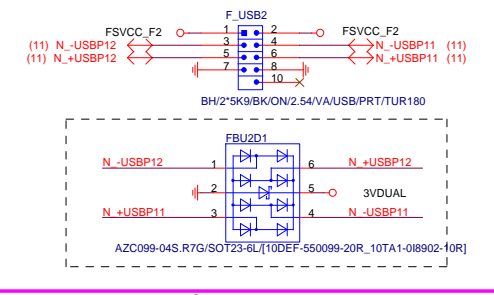
NET 可變



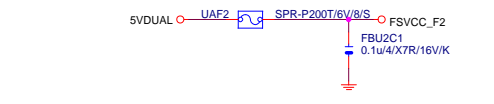
Close to connector
FUSE 2 Port 1 Fuse 2A



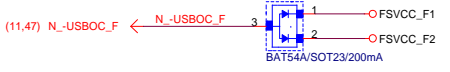
NET 可變



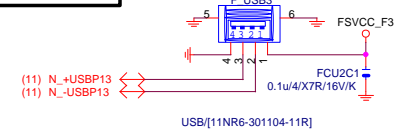
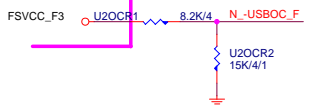
Close to connector
FUSE 2 Port 1 Fuse 2A



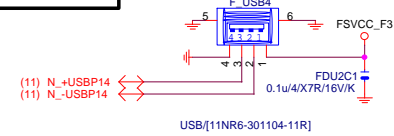
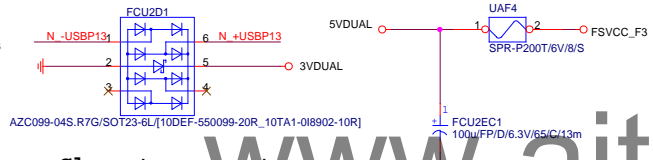
F_USB 2.0 OC SIGNAL



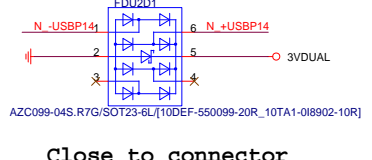
POWER 可自行調整

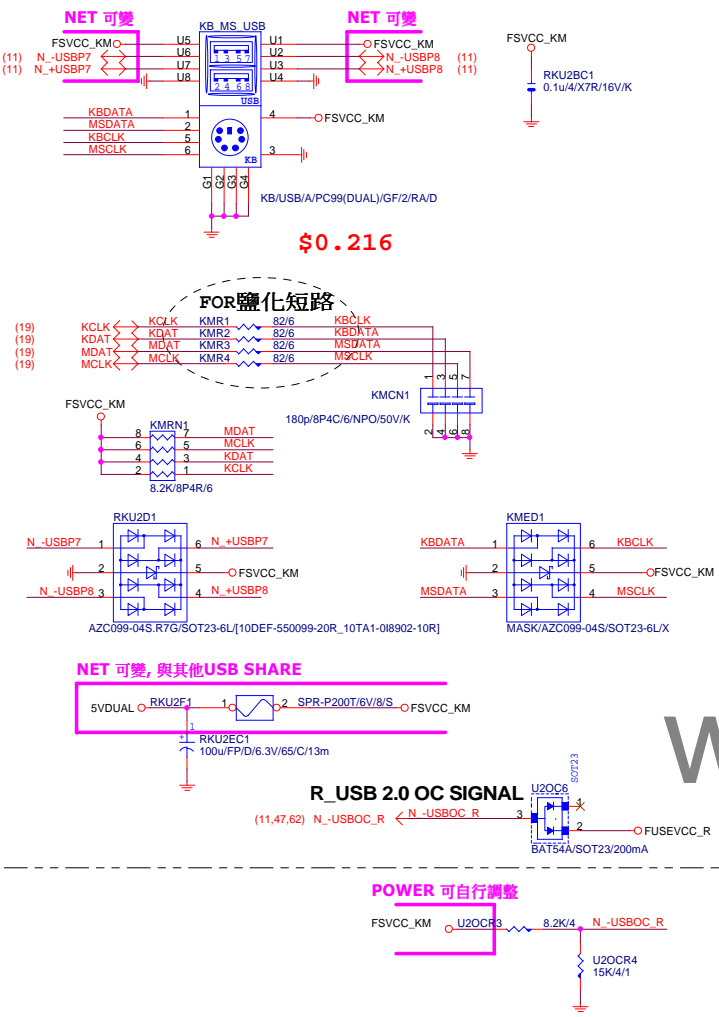


Close to connector

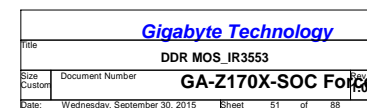


Close to connector

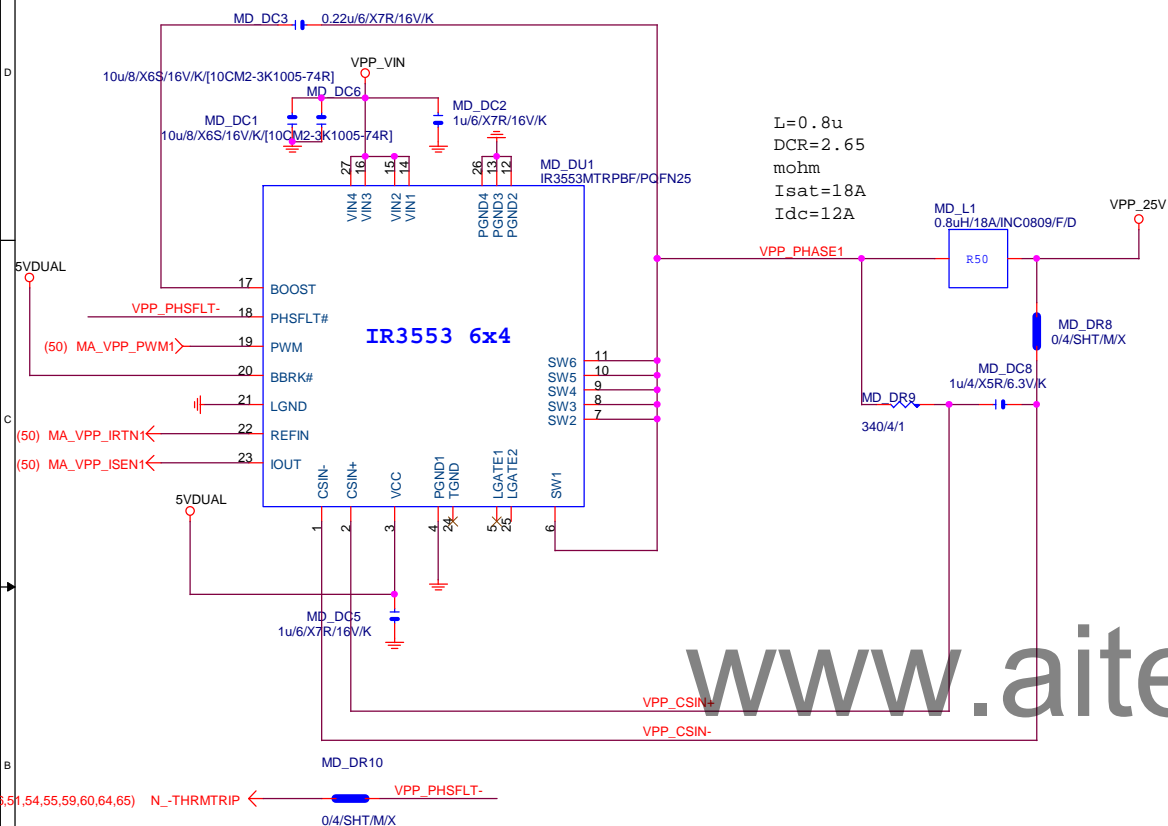




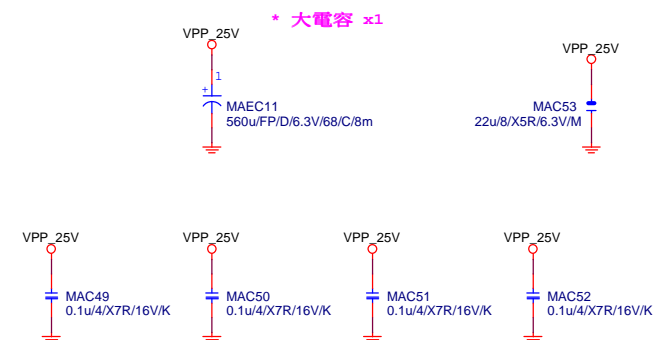
www.aitech1.ru



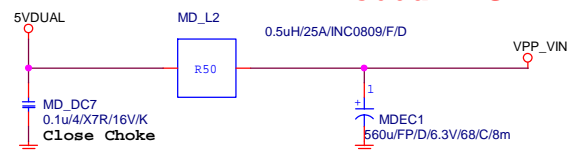
DDR_VPP REV:0.82



VPP CAP 560u*1PCS
22u*1PCS

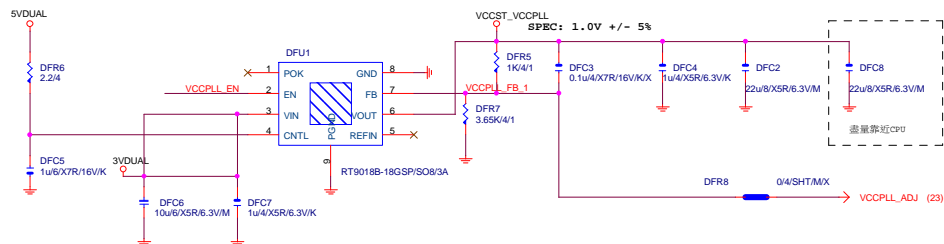


DDR_VPP VIN CAP
560u*1PCS

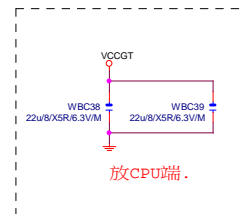
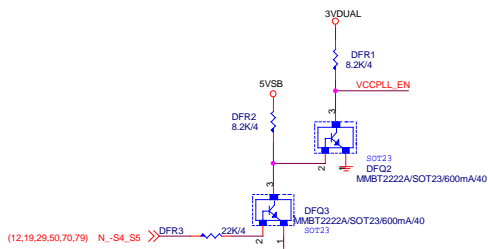


Gigabyte Technology			
Title VPP_MOS IR3553			
Size B	Document Number	GA-Z170X-SOC Force	Rev 1.01
Date:	Wednesday, September 30, 2015	Sheet 52	of 88

VCCST_VCCPLL

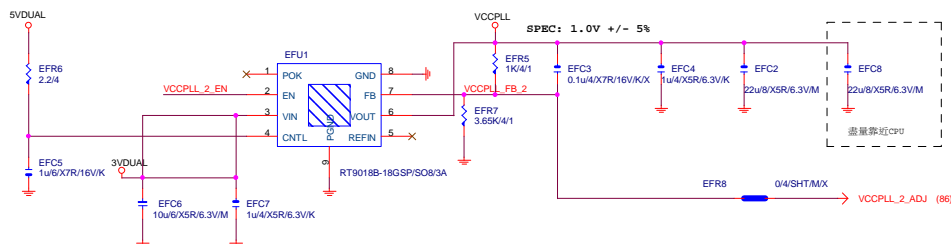


1.0V/ICCMAX:0.11A

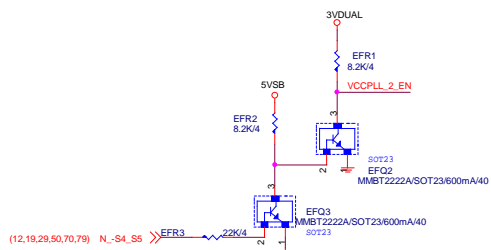


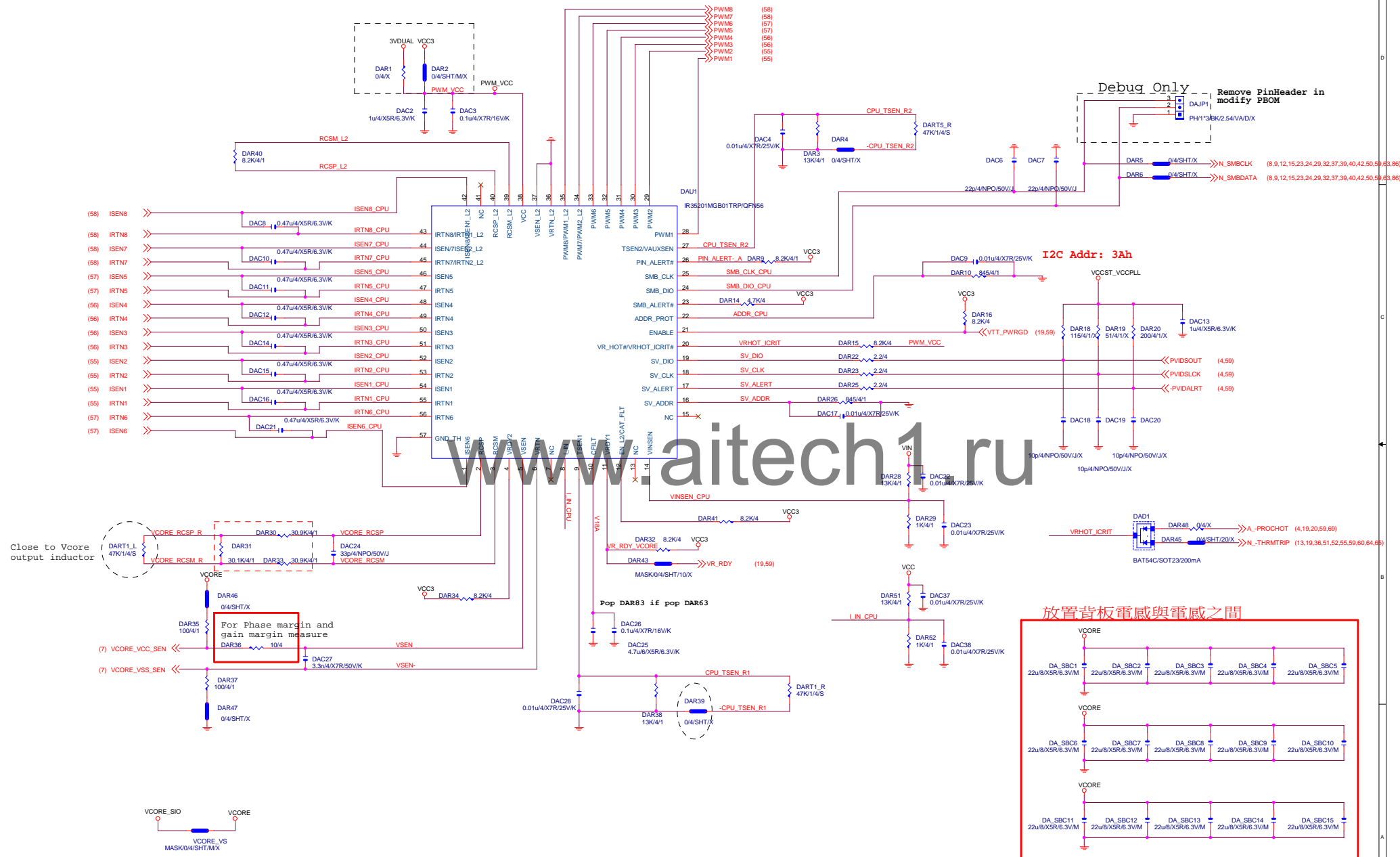
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VCCST_VCCPLL



1.0V/ICCMAX:0.11A

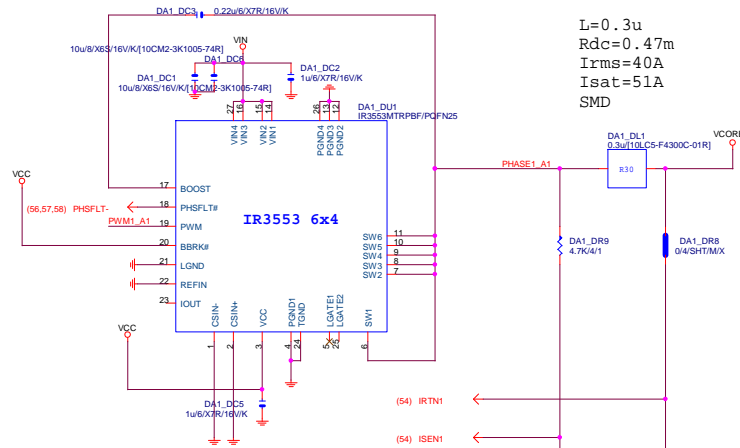




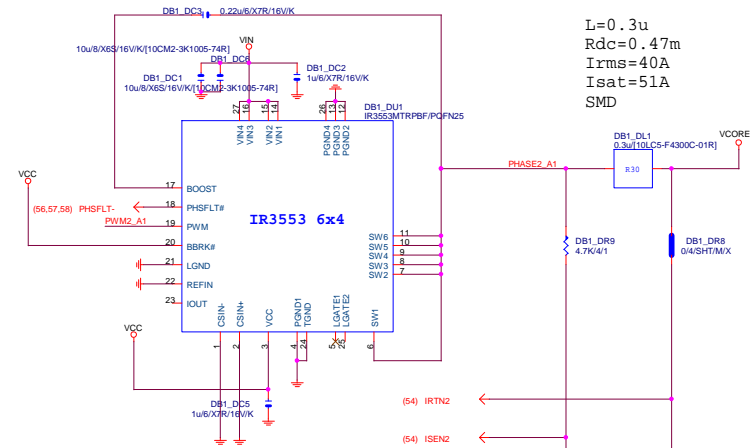
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Title	IR35201_PWM	
Size	Document Number	Rev
Custom	GA-Z170X-SOC Force	1.01
Date	Wednesday, September 30, 2015	Sheet 54 of 88

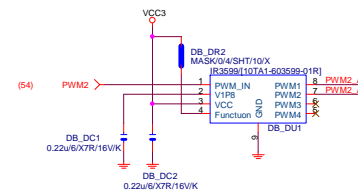
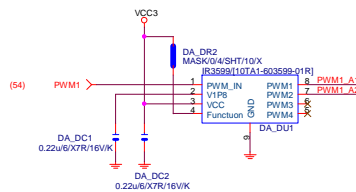
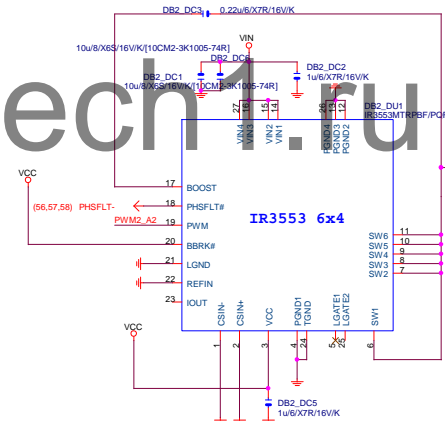
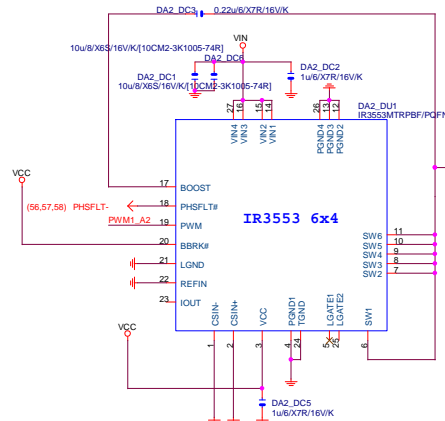
VCORE PHASE1_2



VCORE PHASE3_4



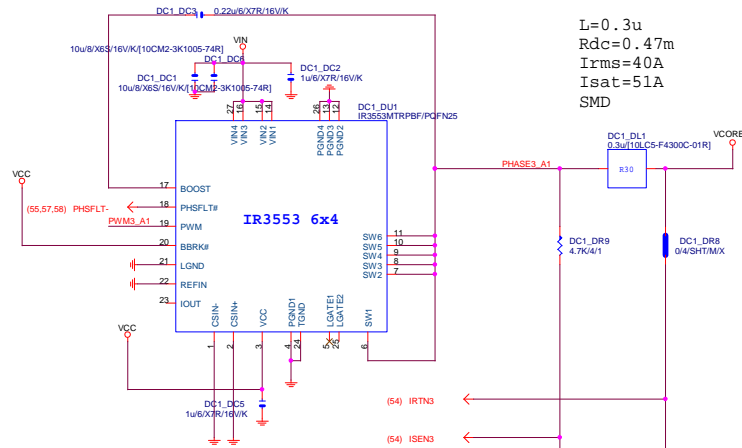
DA_DR1 0/4/SHT/MX PHSFLT- DAR42 8.2K/4/1X VCC



function = 0 --> Quad mode
function = 1 --> Doubled mode

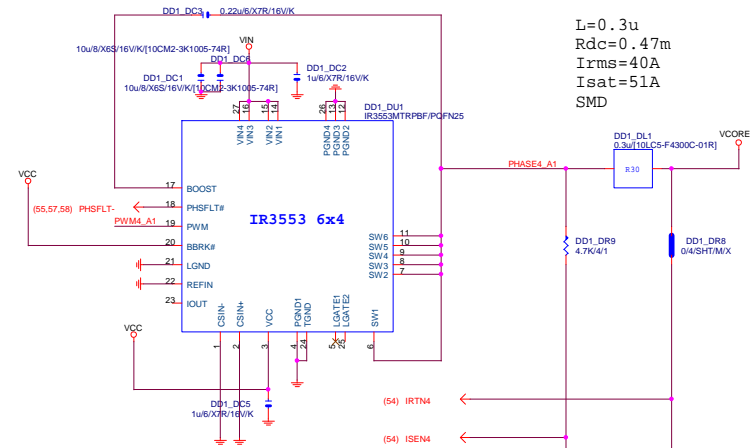
function = 0 --> Quad mode
function = 1 --> Doubled mode

VCORE PHASE5_6

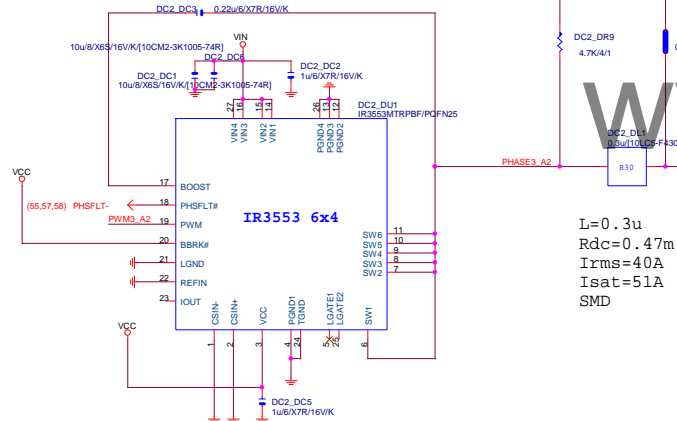


L=0.3u
Rdc=0.47m
Irms=40A
Isat=51A
SMD

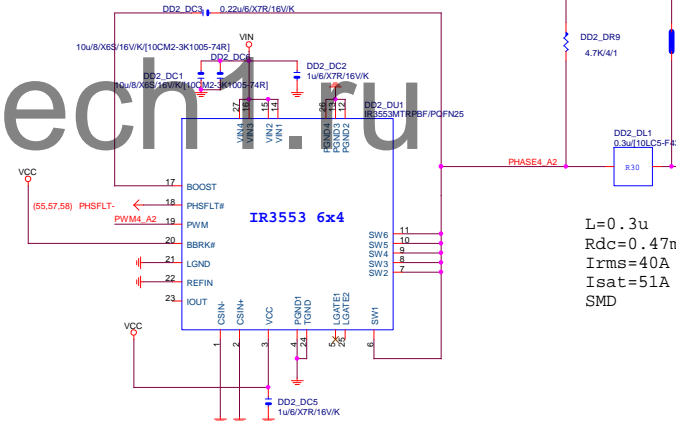
VCORE PHASE7_8



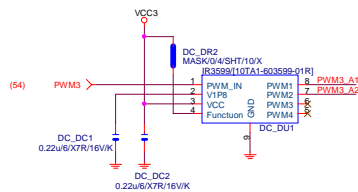
L=0.3u
Rdc=0.47m
Irms=40A
Isat=51A
SMD



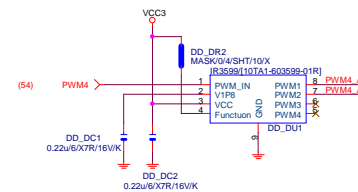
L=0.3u
Rdc=0.47m
Irms=40A
Isat=51A
SMD



L=0.3u
Rdc=0.47m
Irms=40A
Isat=51A
SMD

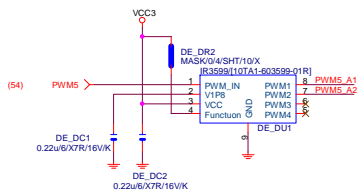
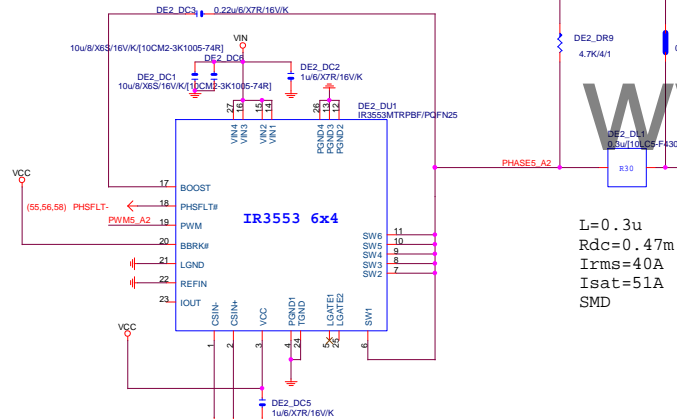
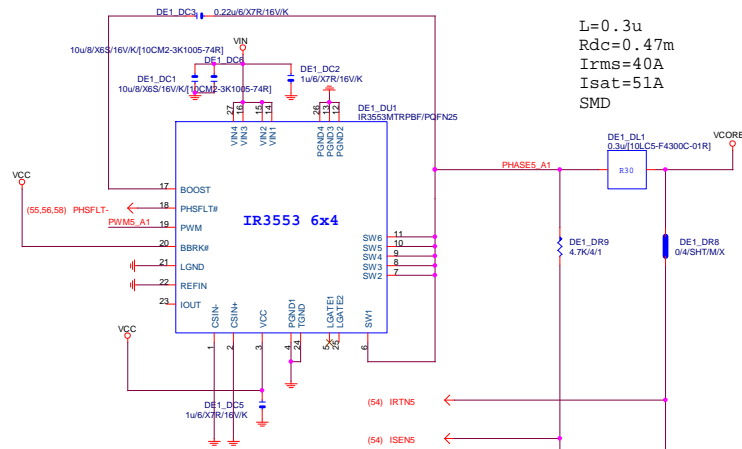


function = 0 --> Quad mode
function = 1 --> Doubled mode



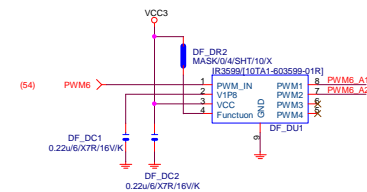
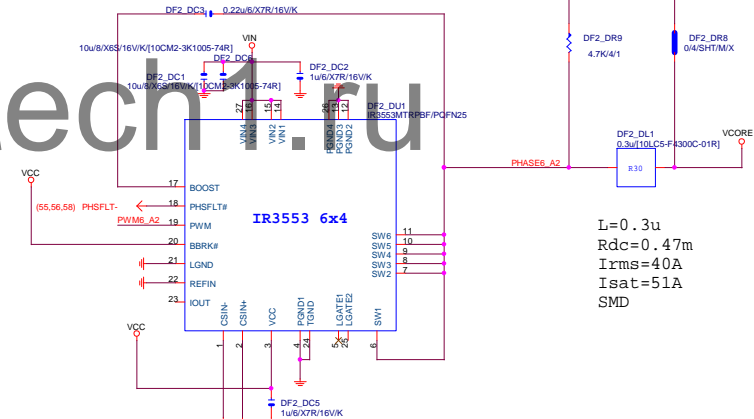
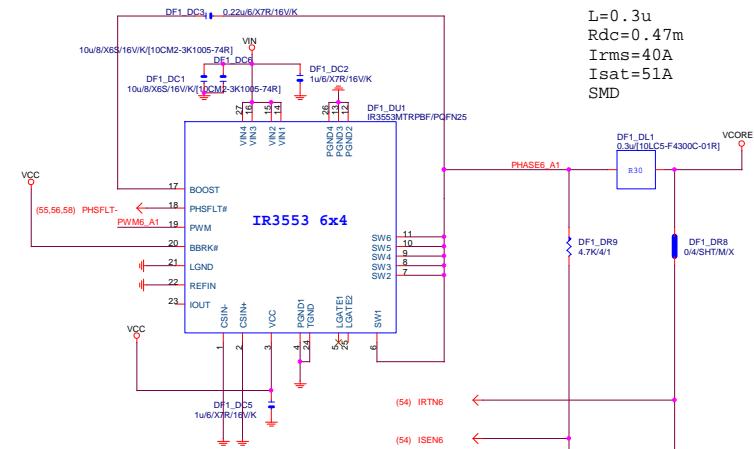
function = 0 --> Quad mode
function = 1 --> Doubled mode

VCORE PHASE9_10



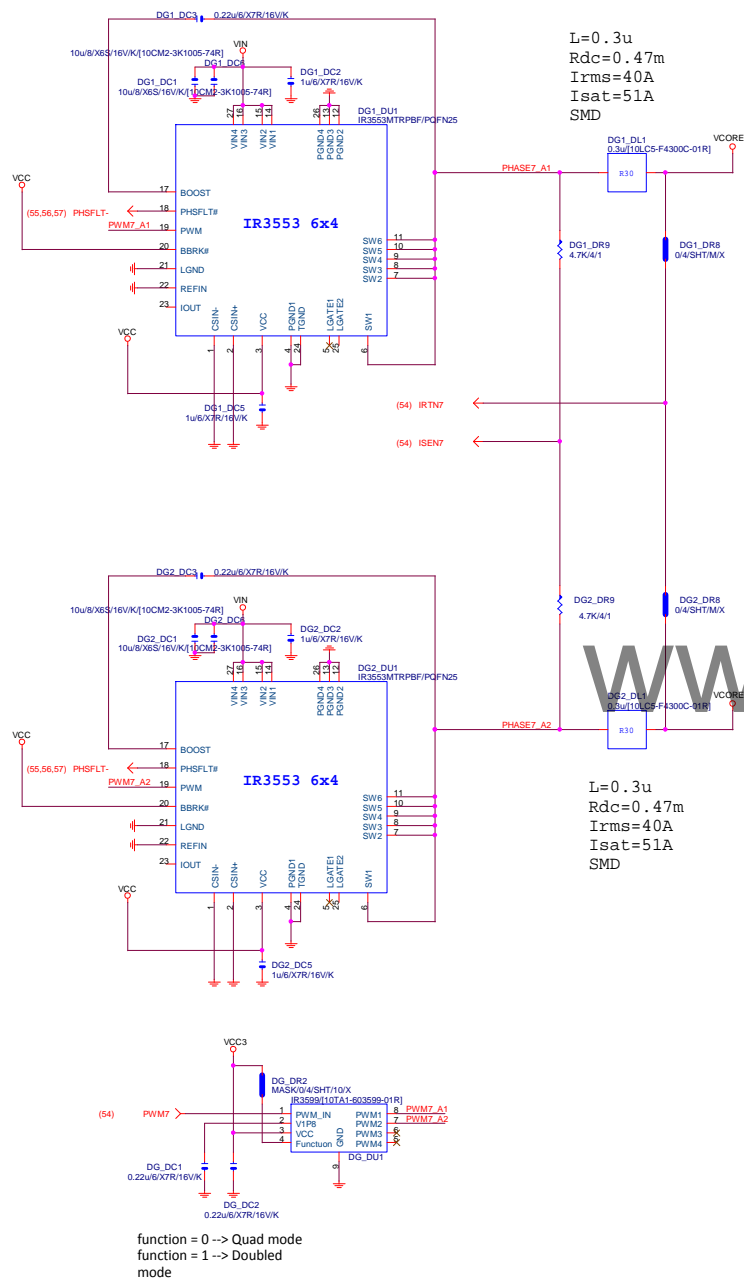
function = 0 --> Quad mode
 function = 1 --> Doubled mode

VCORE PHASE11_12

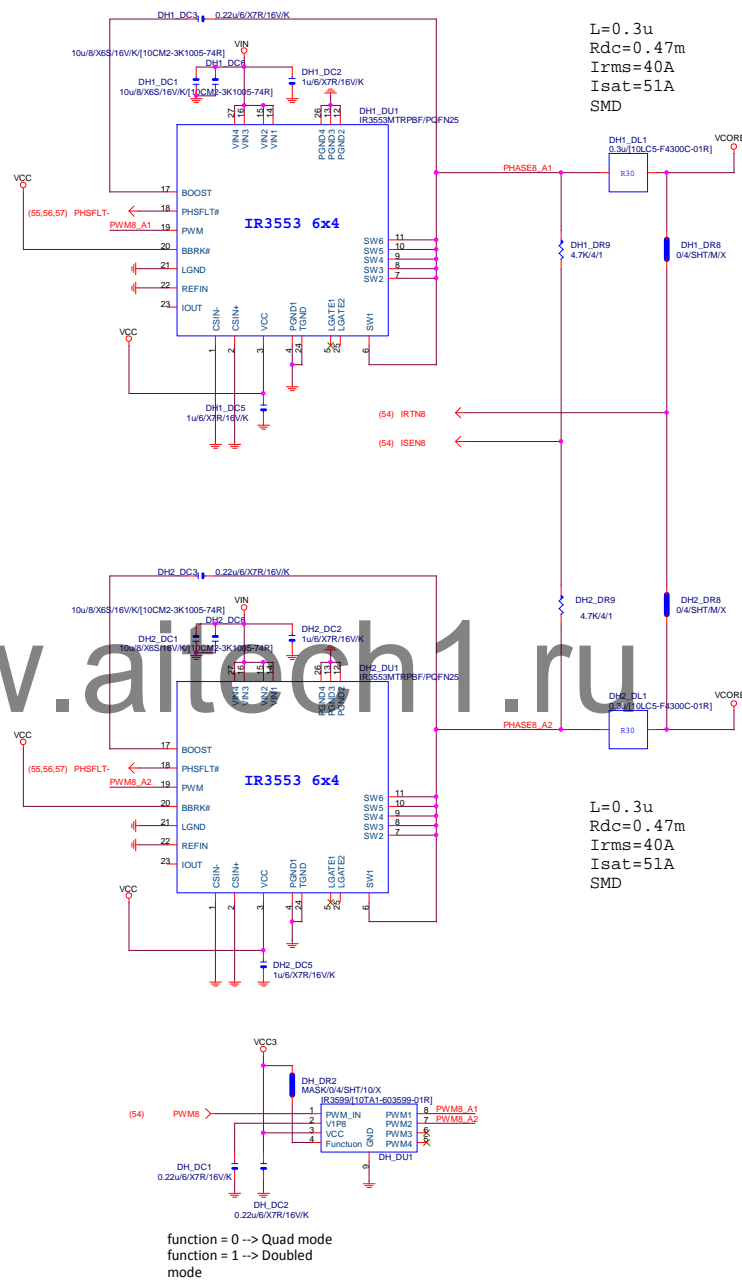
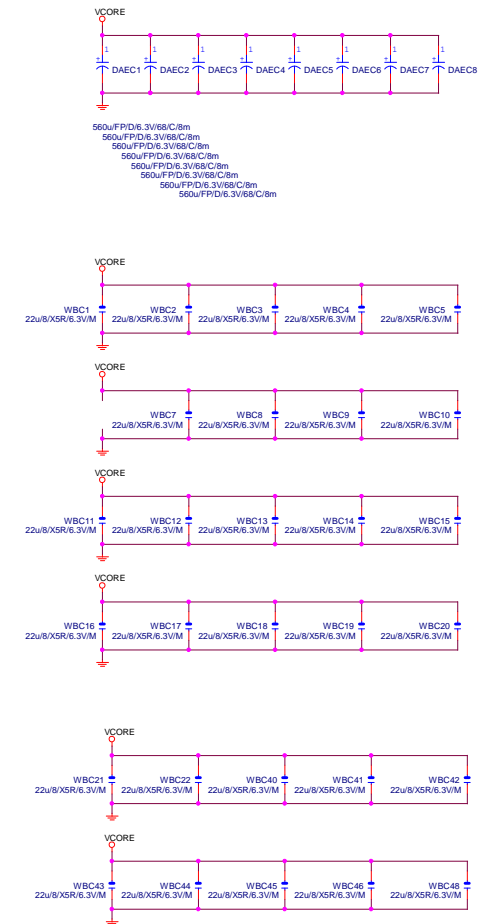


function = 0 --> Quad mode
 function = 1 --> Doubled mode

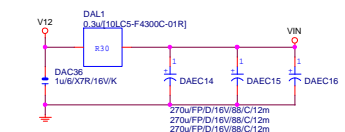
VCORE PHASE13_14

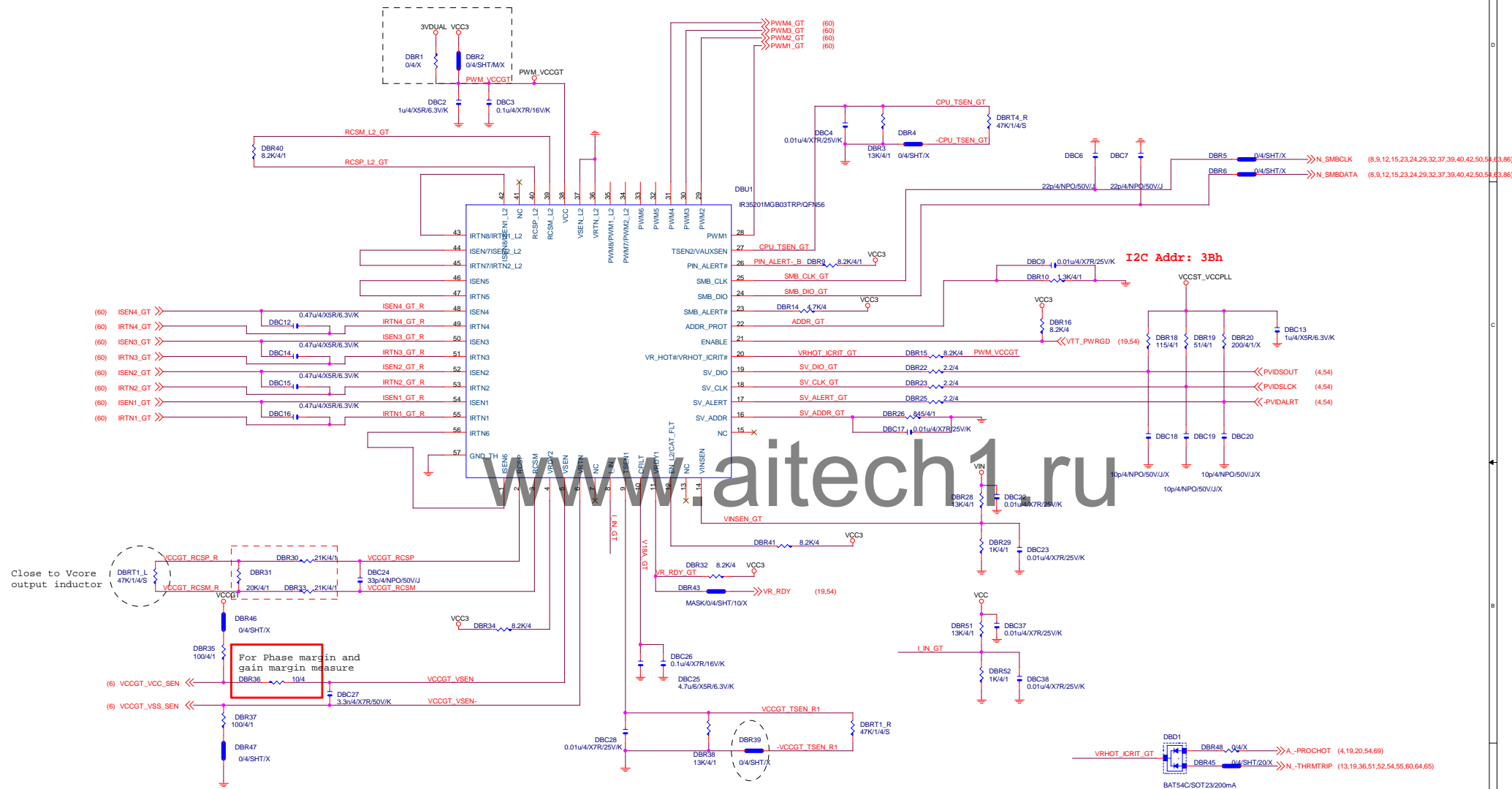


VCORE PHASE15_16

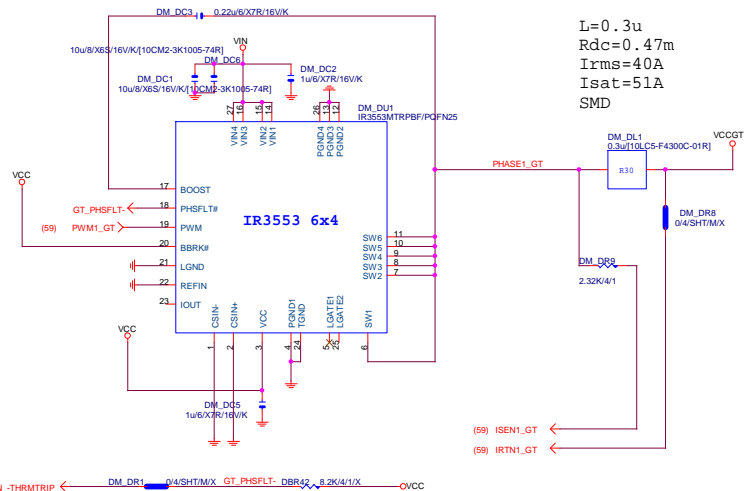
VCORE CAP 560u*8PCS
22u*29PCS

VIN CAP 270u*3PCS

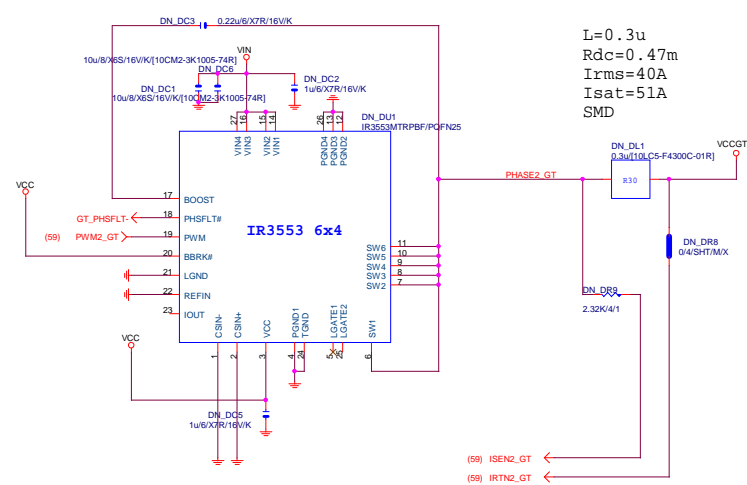




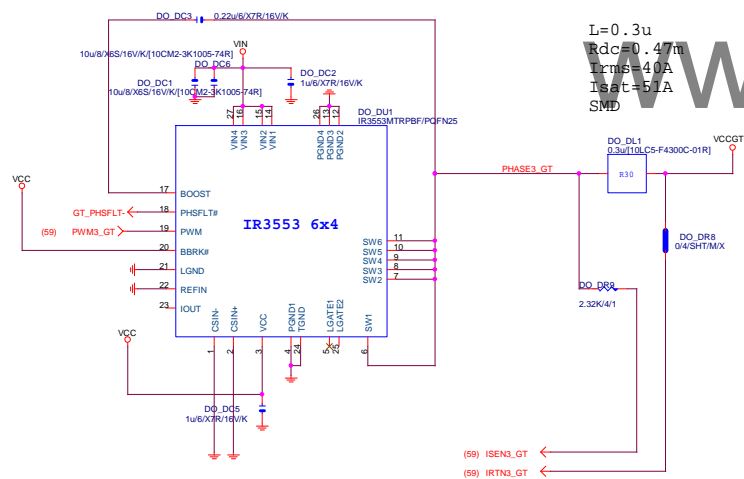
VCCGT-PHASE1



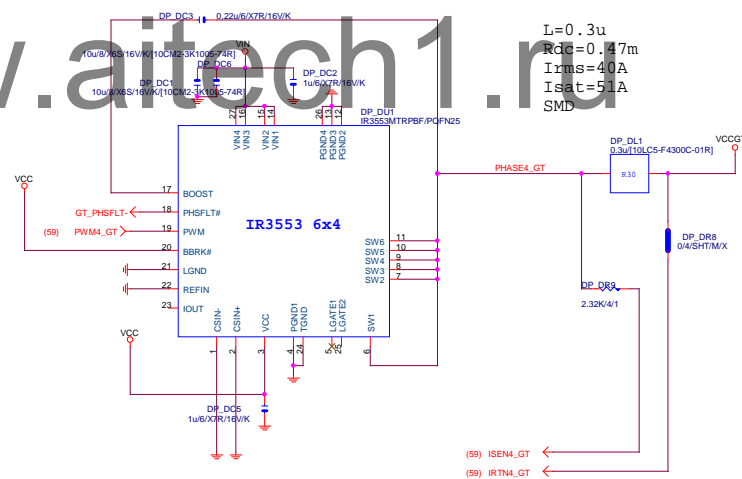
VCCGT-PHASE2



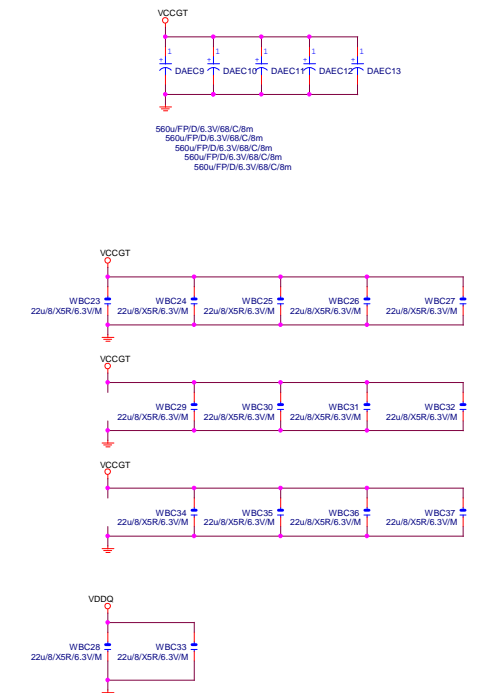
VCCGT-PHASE3



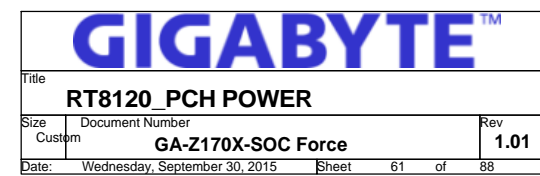
VCCGT-PHASE4



VCCGT CAP 560u*5PCS
22u*15PCS

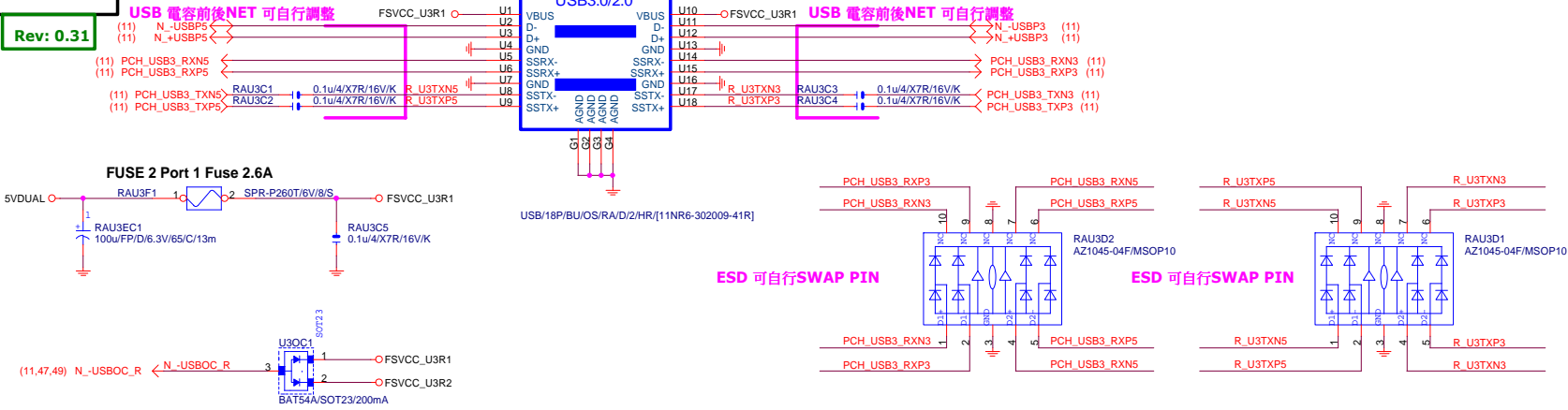


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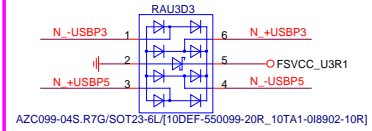


R_USB30_1

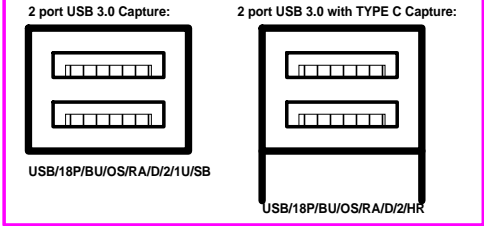
Rev: 0.31



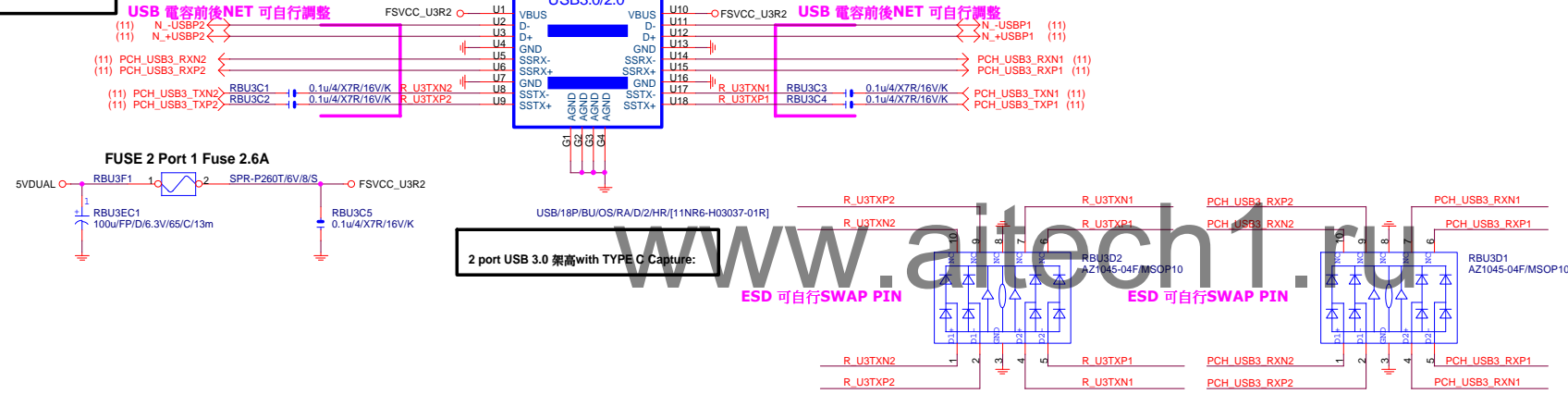
ESD 可自行SWAP PIN



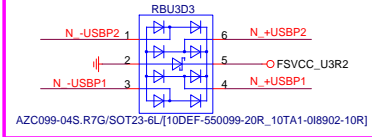
CONNECTOR 自行調整



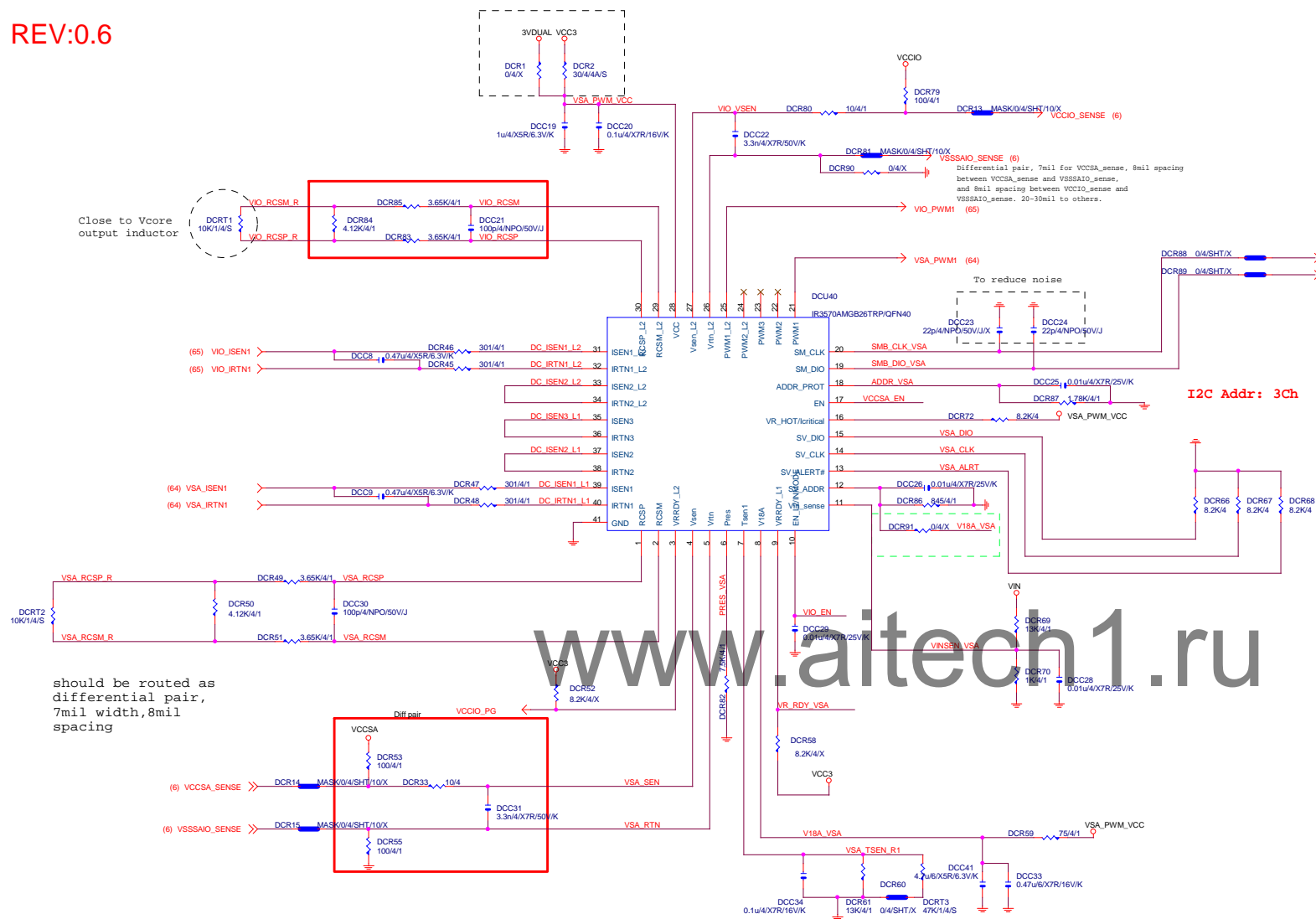
R_USB30_2



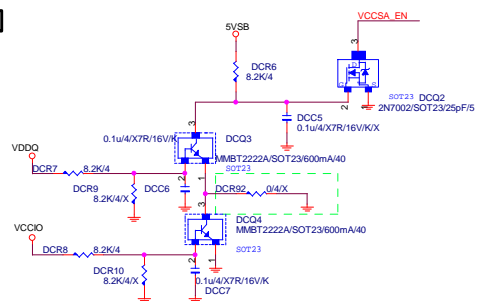
ESD 可自行SWAP PIN



REV:0.6



PWR SEQ



(19) VIO_EN > VIO_EN > DCR5 > 0/4 > VCCIO_EN (19,86)

Connect to IT8620

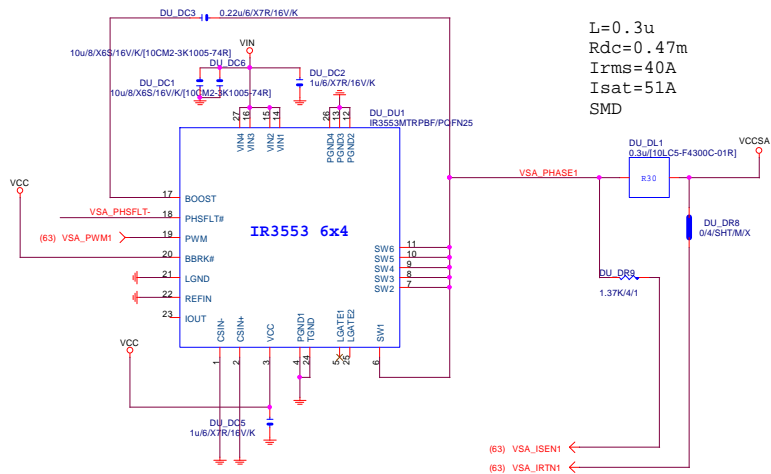


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DDR & VPP POWER IR3570

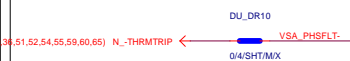
Size	Document Number	Rev
C	GA-Z170X-SOC Force	1.01
Date:	Wednesday, September 30, 2015	Sheet 63 of 88

VCCSA



L=0.3u
Rdc=0.47m
Irms=40A
Isat=51A
SMD

1.05V/ICCMAX:13A




VCCSA CAP 560u*1PCS
22u*1PCS

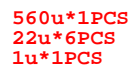


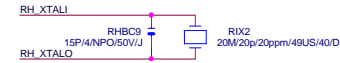
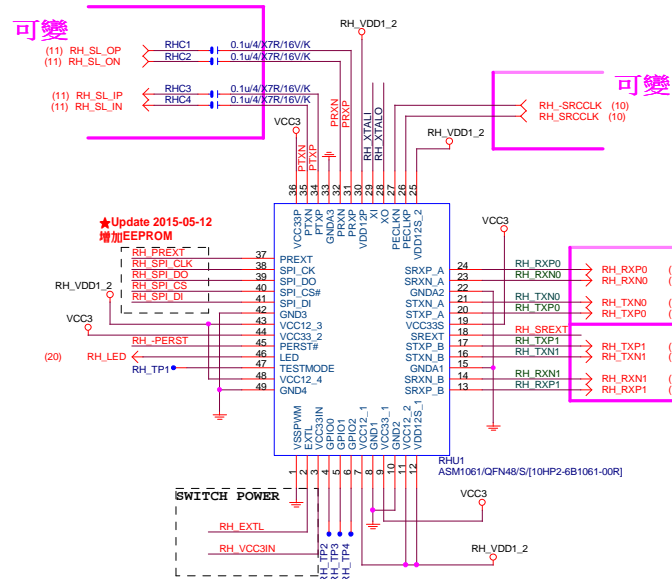
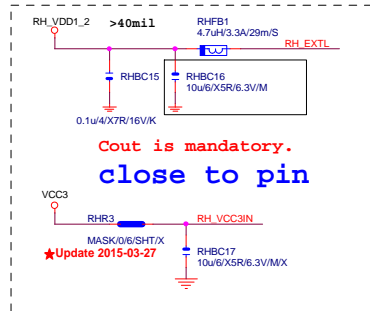
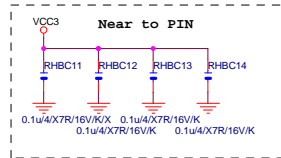
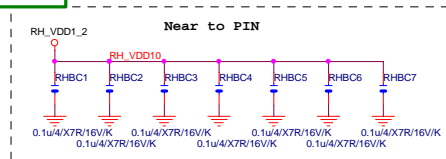
VCCSA
DU_SBC2
1u/4/X5R/6.3V/K

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Title			
DDR MOS_IR3553			
Size	Document Number	GA-Z170X-SOC Force	
Custom			Rev. 1.0
Date:	Wednesday, September 30, 2015	Sheet	64 of 88

VCCIO CAP

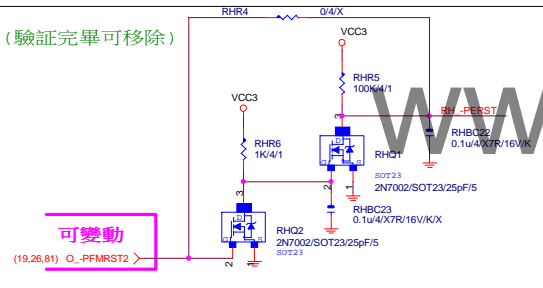




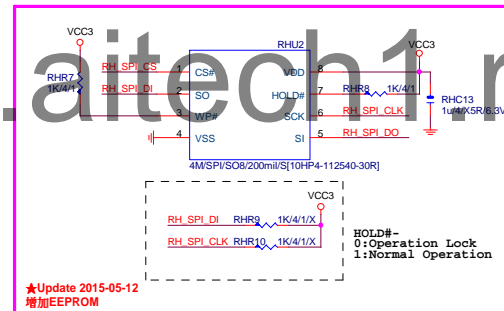
SATA PORT 0

SATA PORT 1

(驗證完畢可移除)

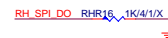


★Update 2015-03-27
移除RH_VDD1_2 external power



H/W Strapping

refer to datasheet:

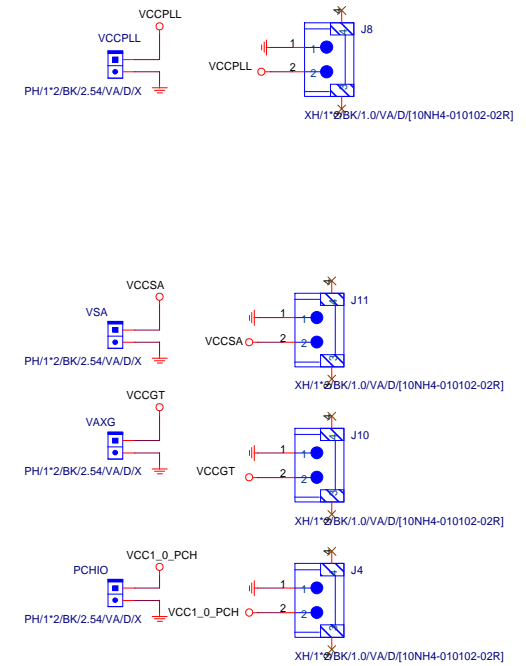
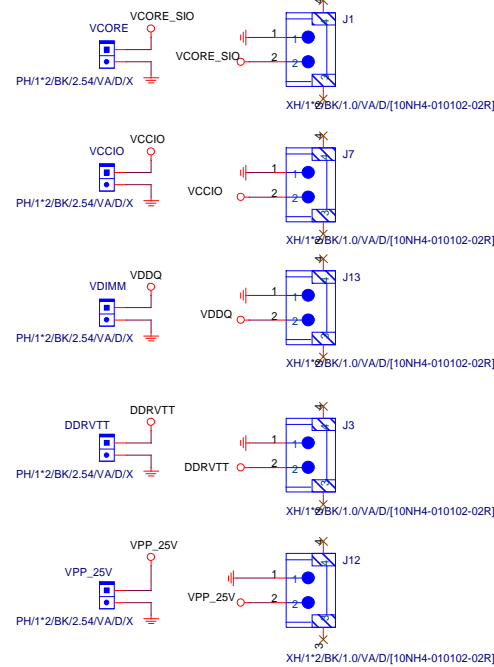


SPI_DO
0: Spin up by H/W
1: Spin up by S/W

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Title			ASM1061
Size	Document Number	Rev	
Custom	GA-Z170X-SOC Force	1.01	
Date:	Wednesday, September 30, 2015	Sheet	66 of 88

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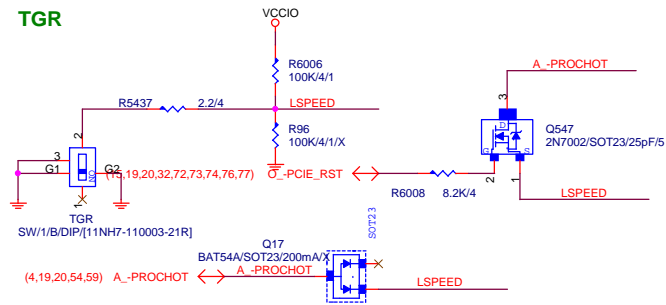


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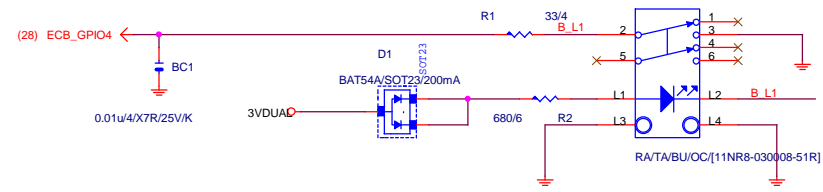
OC BOTTOMGA-Z170X-SOC Force Rev 1.01

TGR



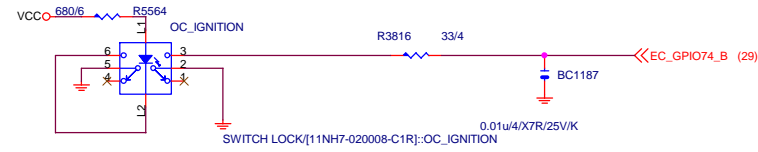
OCPSW

IT8951:GPIO4



EnPWR BUTTON

IT8792:GPIO74



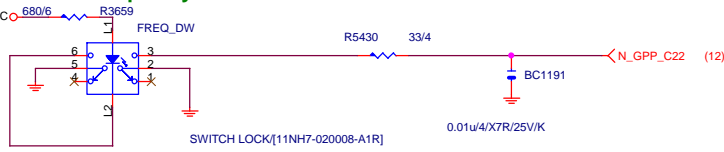
Frequency Up

PCH:GPP_C23



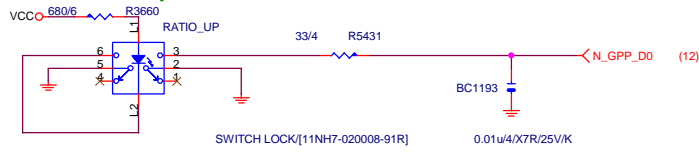
Frequency Down

PCH:GPP_C22



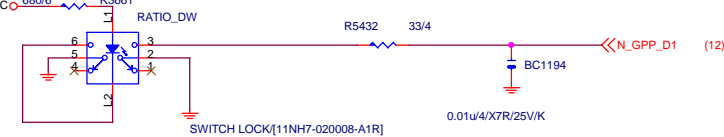
Ratio Up

PCH:GPP_D0



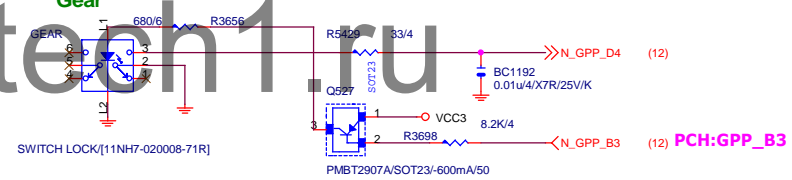
Ratio Down

PCH:GPP_D1



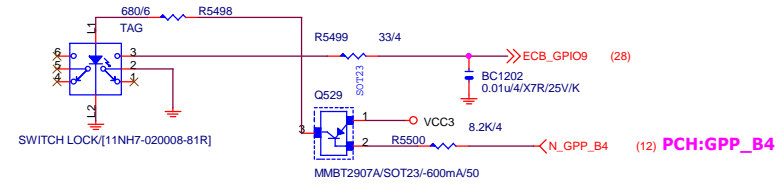
Gear

PCH:GPP_D4



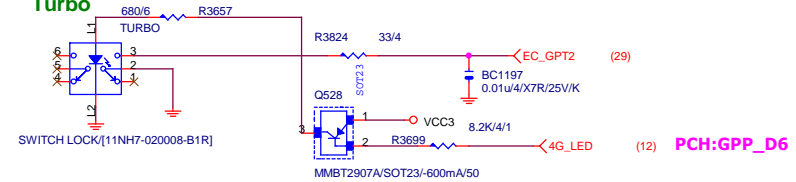
TAG BUTTON

IT8951:GPIO9



Turbo

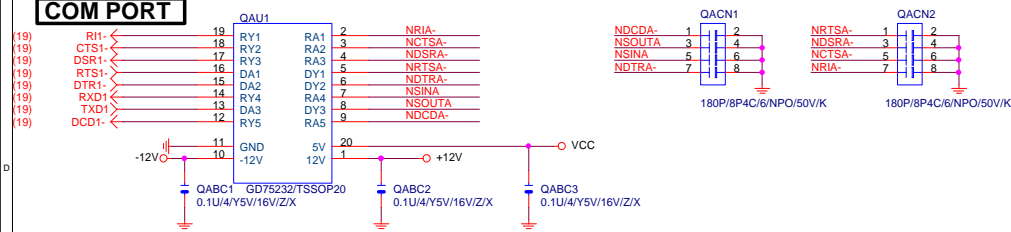
IT8792:GPIO72



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Title SWITCH		
Size Custom	Document Number GA-Z170X-SOC Force	Rev 1.01
Date: Wednesday, September 30, 2015	Sheet 69	of 88

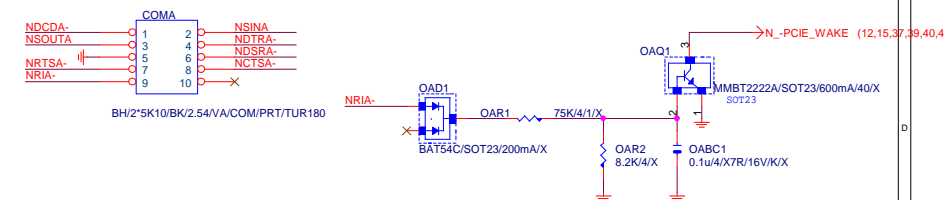
COM PORT



Rev: 0.7

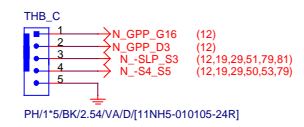
LPT PORT

COMA



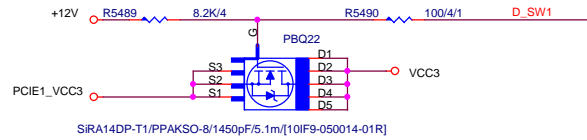
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Thunderbolt

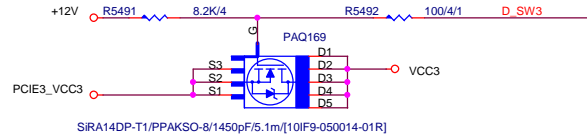


Gigabyte Technology			
Title			
FP,F_USB,USB PWR,BZ			
Size	Document Number	GA-Z170X-SOC For	
Custom		Rev 1.01	
Date:	Wednesday, September 30, 2015	Sheet	70 of 88

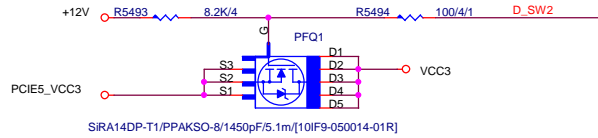
PCIEX16_1



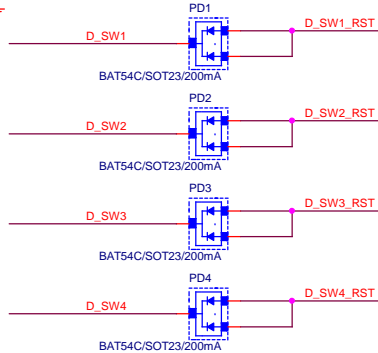
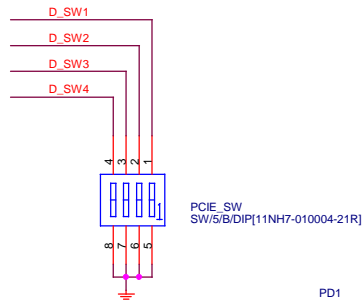
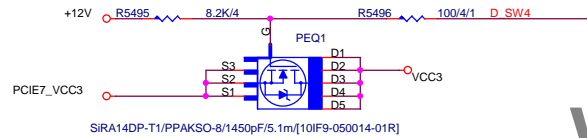
PCIEX16_2



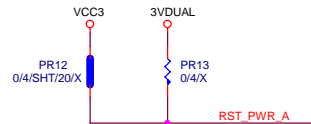
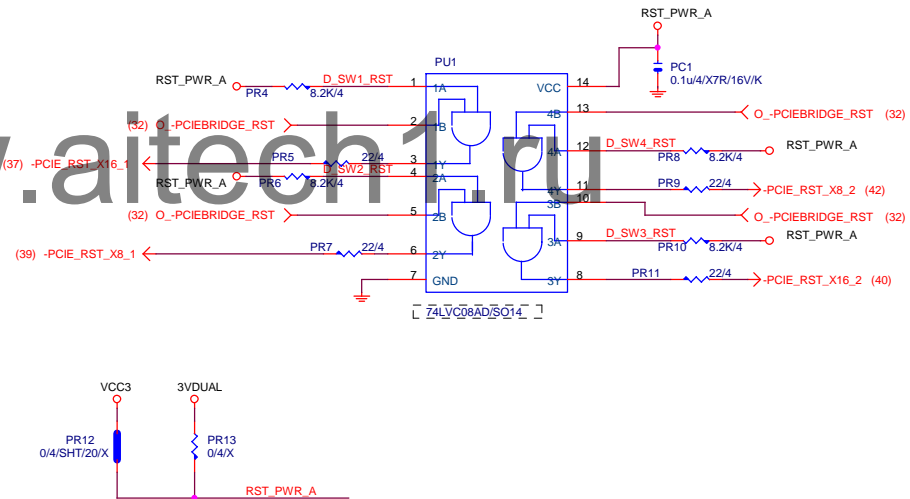
PCIEX8_1



PCIEX8_2



DIMM_SW



GIGABYTE™			
Title SWITCH			
Size Custom	Document Number GA-Z170X-SOC Force	Rev 1.01	
Date: Wednesday, September 30, 2015	Sheet 71	of 88	

M.2 Lane4 from PCH port18

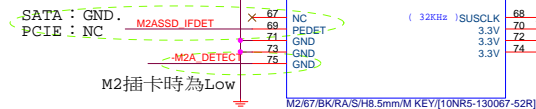
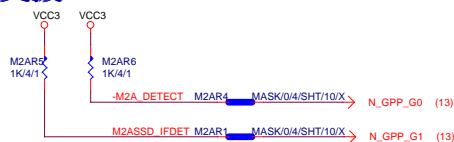
M.2 Lane3 from PCH port17

M.2 Lane2 from PCH port16

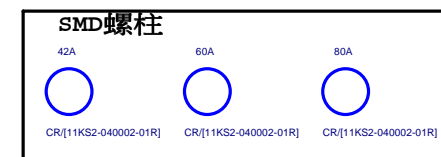
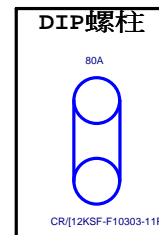
M.2 Lane2 from PCH port15

需與M2_-CLKREQ對應

支援SATA and M.2 function



M.2 有插卡 /沒插卡 GPP_G0	M.2插何種卡? GPP_G1	SATA Express 插何種硬碟? GPP_E0/E2/F1	IO15 (S0)	IO16 (S1)	IO17	IO18	IO19 (S0)	IP20 (S1)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (M.2)	PCIE x1	PCIE x1	PCIE X1	PCIE x1	SATA
		SATA Express (Low)	SATA (M.2)	PCIE x1	PCIE x1	PCIE x1	SATA Express	
	PCIE Mode (Hi)	SATA (Hi)	PCIE x4 (For M.2)				SATA	SATA
		SATA Express (Low)	PCIE x4 (For M.2)				SATA Express	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	PCIE x4				SATA	SATA
		SATA Express (Low)	PCIE x4				SATA Express	



M.2 Lane2 from PCH port19

(75) M2_PCIE_IN13 < 0.22u/4/X5R/6.3V/K M2DC15
(75) M2_PCIE_IP13 < 0.22u/4/X5R/6.3V/K M2DC16

M.2 Lane2 from PCH port20

(75) M2_PCIE_IN14 < 0.22u/4/X5R/6.3V/K M2DC3
(75) M2_PCIE_TP14 < 0.22u/4/X5R/6.3V/K M2DC16

M.2 Lane3 from PCH port21

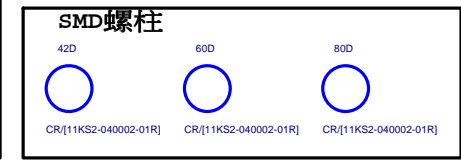
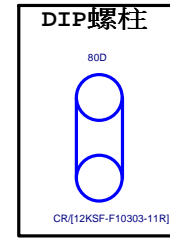
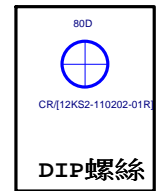
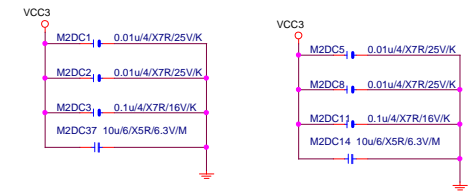
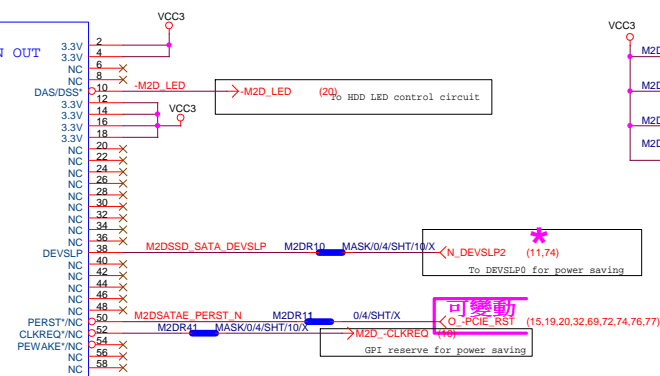
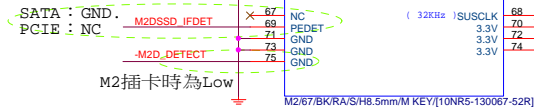
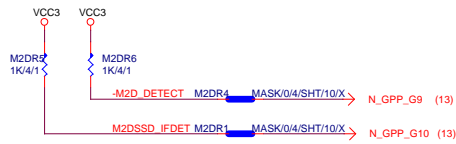
(75) M2_PCIE_IN15 < 0.22u/4/X5R/6.3V/K M2DC35
(75) M2_PCIE_IP15 < 0.22u/4/X5R/6.3V/K M2DC36

M.2 Lane4 from PCH port22

(75) M2_PCIE_IP16 < 0.22u/4/X5R/6.3V/K M2DC33
(75) M2_PCIE_TP16 < 0.22u/4/X5R/6.3V/K M2DC34

(10) CK_M2D_100M_DN
(10) CK_M2D_100M_DP
需與M2_-CLKREQ對應

支援SATA and M.2 function



M.2-SATA(S3)+SATA S0&S1&S2

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	H (SATA)	GPP_C21	H

M.2X4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	H
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	N/A	GPP_C21	H

M.2沒插卡+SATA S0~S3

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	H	GPP_C21	L

M.2 插卡 / 沒插卡	M.2 插卡? GPP_G9	SATA Express 有何插板? GPP_E0/E1/E2/F0	I019 (S0)	I020 (S1)	I021 (S2)	I022 (S3)
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA	SATA	SATA	SATA (For M2)
		SATA Express (Low)	SATA Express (For S.E.0)	SATA	SATA (For M2)	
沒插卡 (Hi)	PCIE Mode (Hi)	SATA (Hi)	PCIEx4 (For M.2)			
		SATA Express (Low)	PCIEx4 (For M.2)			
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	SATA (S0)	SATA (S1)	SATA (S2)	SATA (S3)
		SATA Express (Low)	SATA Express (For S.E.0)	SATA Express (For S.E.1)	SATA Express (For S.E.1)	

M.2-SATA(S3)+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	L	GPP_C19	L
GPP_E0/E1/E2/F0	L (S.E.)	GPP_C21	H

M.2X2+S.E.D(S0+S1)

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	L	GPP_C21	H

M.2沒插卡+S.E.C&S.E.D

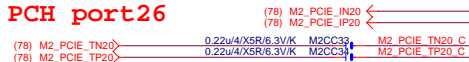
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	H	GPP_C20	L
GPP_G10	H	GPP_C19	L
GPP_E0/E1/E2/F0	L	GPP_C21	L

M.2X2+SATA S0&S1

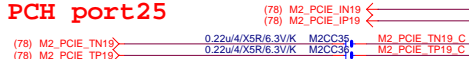
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G9	L	GPP_C20	L
GPP_G10	H	GPP_C19	H
GPP_E0/E1/E2/F0	H	GPP_C21	H

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M.2 X4			
Size Custom	Document Number	GA-Z170X-SOC Force	
Date: Wednesday, September 30, 2016	Sheet 73 of 88	Rev 1.01	

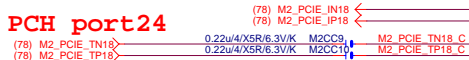
M.2 Lane4 from PCH port26



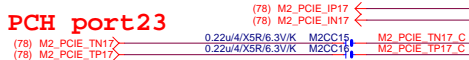
M.2 Lane3 from PCH port25



M.2 Lane2 from PCH port24

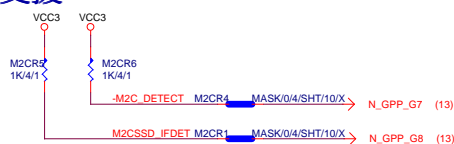


M.2 Lane2 from PCH port23



(10) CK_M2C_100M_DN
(10) CK_M2C_100M_DP
需與M2_-CLKREQ對應

支援SATA and M.2 function



M.2-SATA(S4)+SATA S5

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	L	GPP_C12	H
GPP_G8	L	GPP_C14	L
GPP_F1/F2	H (SATA)	GPP_C13	H
		GPP_C15	L

M.2X4

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	L	GPP_C12	H
GPP_G8	H	GPP_C14	H
GPP_F1/F2	H	GPP_C13	H
		GPP_C15	L

M.2X2+S.E.

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	L	GPP_C12	L
GPP_G8	H	GPP_C14	L
GPP_F1/F2	L	GPP_C13	L
		GPP_C15	H

M.2X2+SATA S4&S5

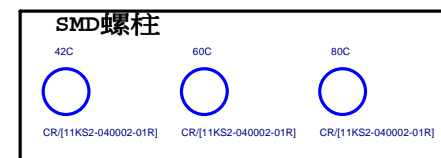
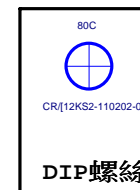
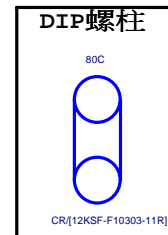
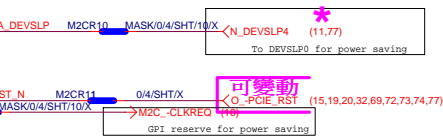
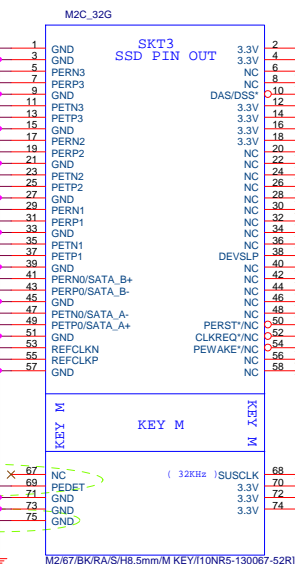
WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	L	GPP_C12	L
GPP_G8	H	GPP_C14	L
GPP_F1/F2	H	GPP_C13	L
		GPP_C15	H

M.2沒插卡+SATA S4&S5

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	H	GPP_C12	L
GPP_G8	H	GPP_C14	L
GPP_F1/F2	H	GPP_C13	L
		GPP_C15	H

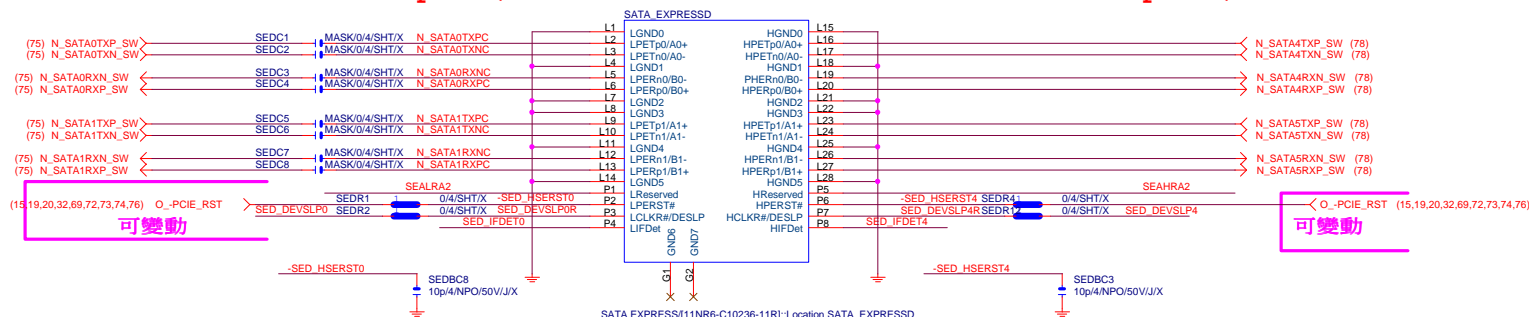
M.2沒插卡+S.E.

WHEN	PCH GPIO	SETUP	SWITCH
GPP_G7	H	GPP_C12	L
GPP_G8	H	GPP_C14	L
GPP_F1/F2	L	GPP_C13	L
		GPP_C15	H



M.2 有插卡 / 沒插卡?	M.2插何種卡? GPP_G10	SATA Express 插何種硬碟? GPP_E0/E1/E2/F0	IO23 (S4)	IO24 (S5)	IO25	IO26
有插卡 (Low)	SATA Mode (Low)	SATA (Hi)	SATA (For M2)	SATA (S5)	PCIEx2	
		SATA Express (Low)	SATA (For M2)	SATA (S5)	PCIEx2	
	PCIe Mode (Hi)	SATA (Hi)	PCIEx4 (For M.2)			
		SATA Express (Low)	SATA Express (For S.E.)		PCIEx2 (For M.2)	
沒插卡 (Hi)	Don't Care (Hi)	SATA (Hi)	SATA (S4)	SATA (S5)	PCIEx2	
		SATA Express (Low)	SATA Express (For S.E)		PCIEx2	

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Title	M.2 X4		
Size	Document Number	Rev	1.01
Custom	GA-Z170X-SOC Force		
Date:	Wednesday, September 30, 2015	Sheet	76 of 88

SATA EXPRESS 下層 To SATA3
port0/1SATA EXPRESS 上層 To SATA3
port4/5

可變動

可變動

SATA EXPRESS[11NR6-C10236-11R]:Location SATA_EXPRESSD

* check
文字面 01/23/45
NET (45/23/01)

SATA EXPRESS料號

雙層:TBD

單層+2SATA:11NR6-C10236-03R

單層:11NR6-C10118-03R

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SATA 5 (文字面寫SATA 1)
SATA 4 (文字面寫SATA 0)
SATA 3
SATA 2
SATA 1 (文字面寫SATA 5)
SATA 0 (文字面寫SATA 4)

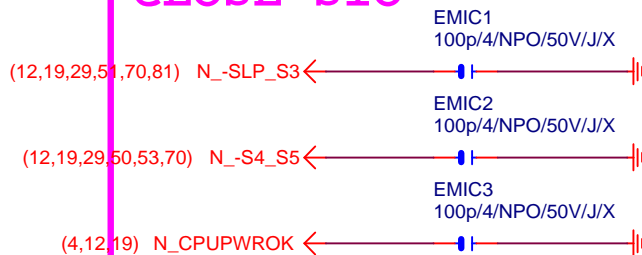
GIGABYTE Technology

SATA EXPRESS

Size Custom Document Number GA-Z170X-SOC Force Rev 1.01

Date: Wednesday, September 30, 2015 Sheet 77 of 88

CLOSE SIO



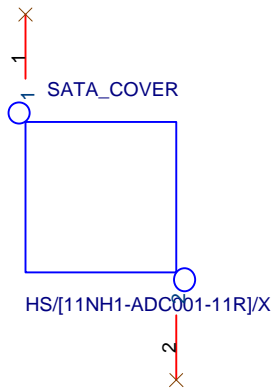
CLOSE PCH



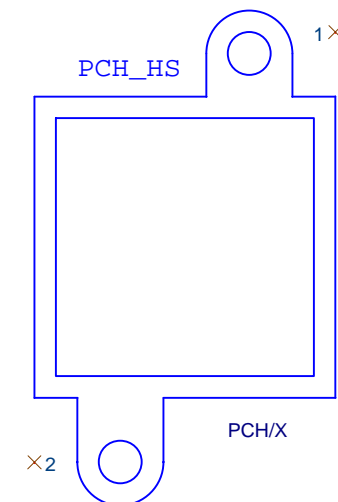
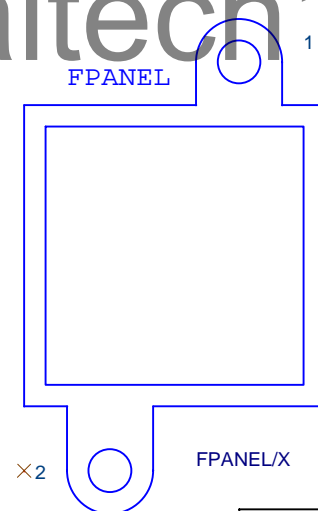
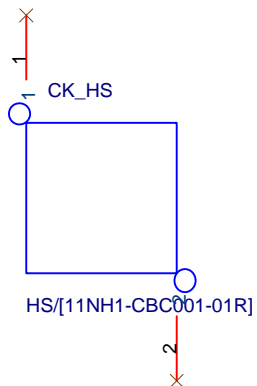
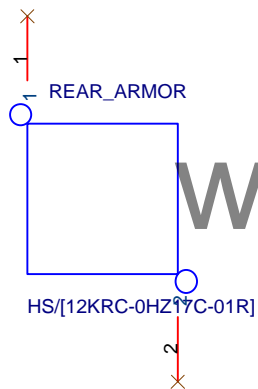
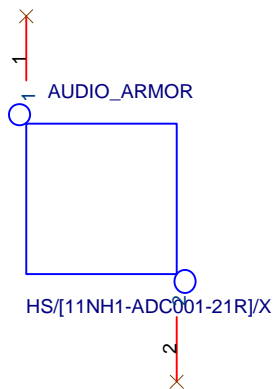
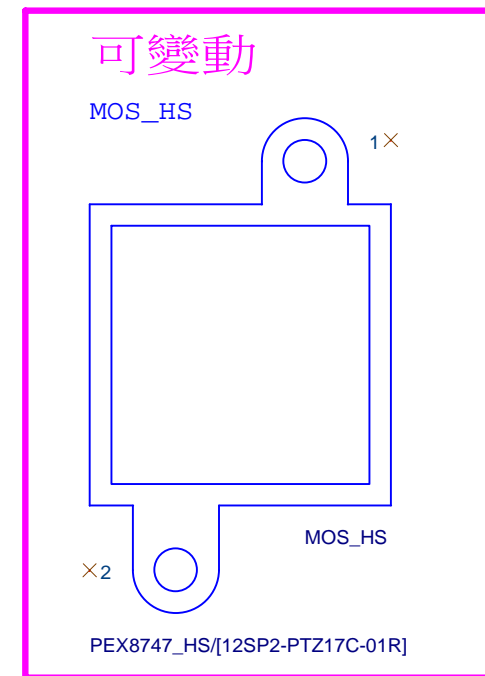
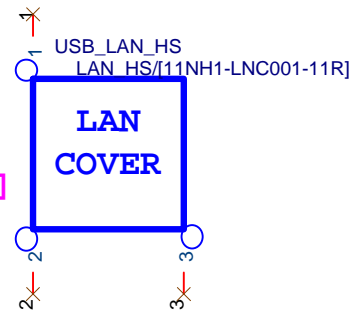
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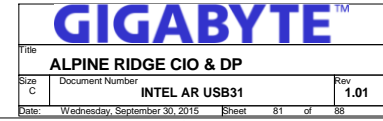
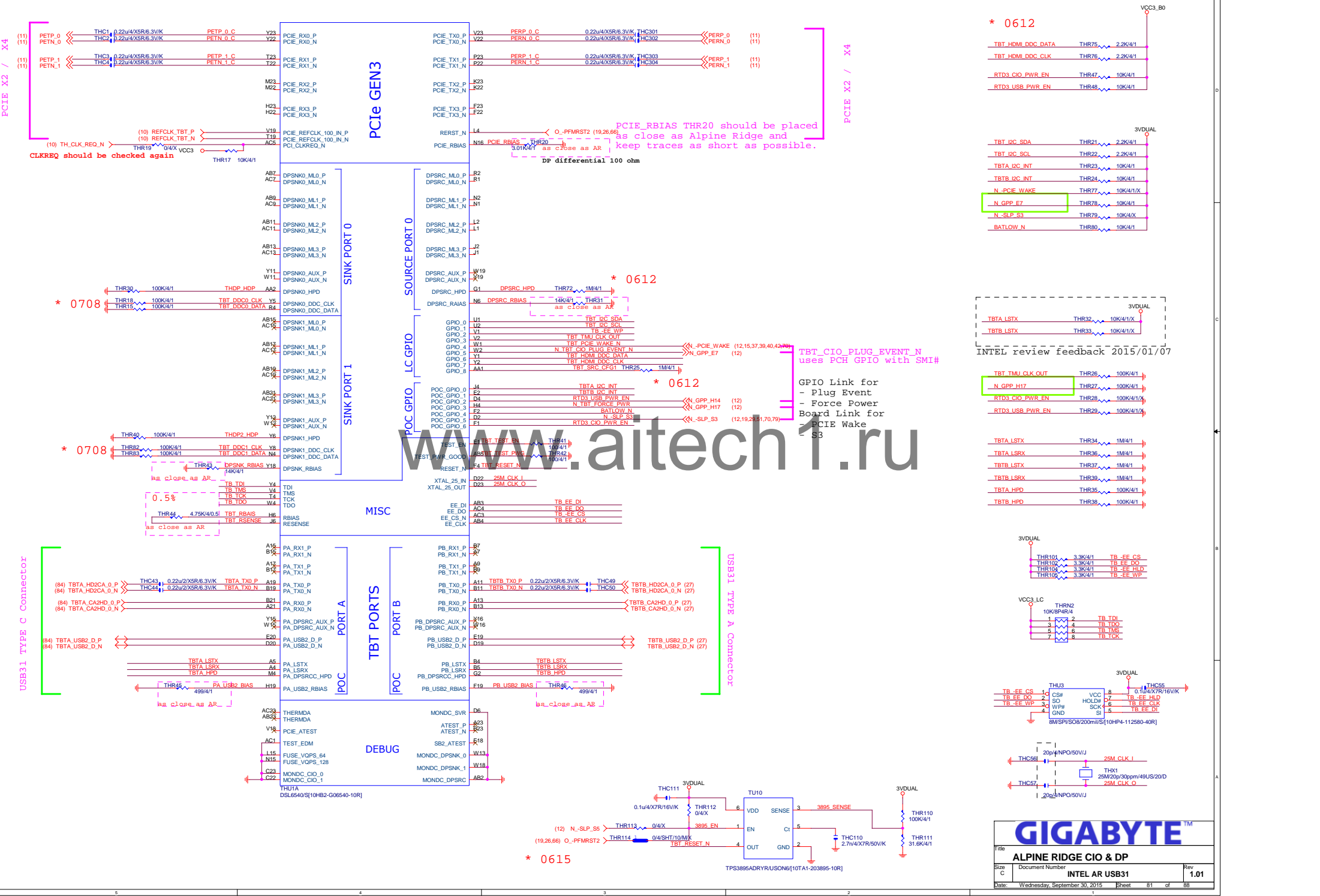
Title		
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Size A	Document Number GA-Z170X-SOC Force	Rev 1.01
Date:	Wednesday, September 30, 2015	Sheet 79 of 88



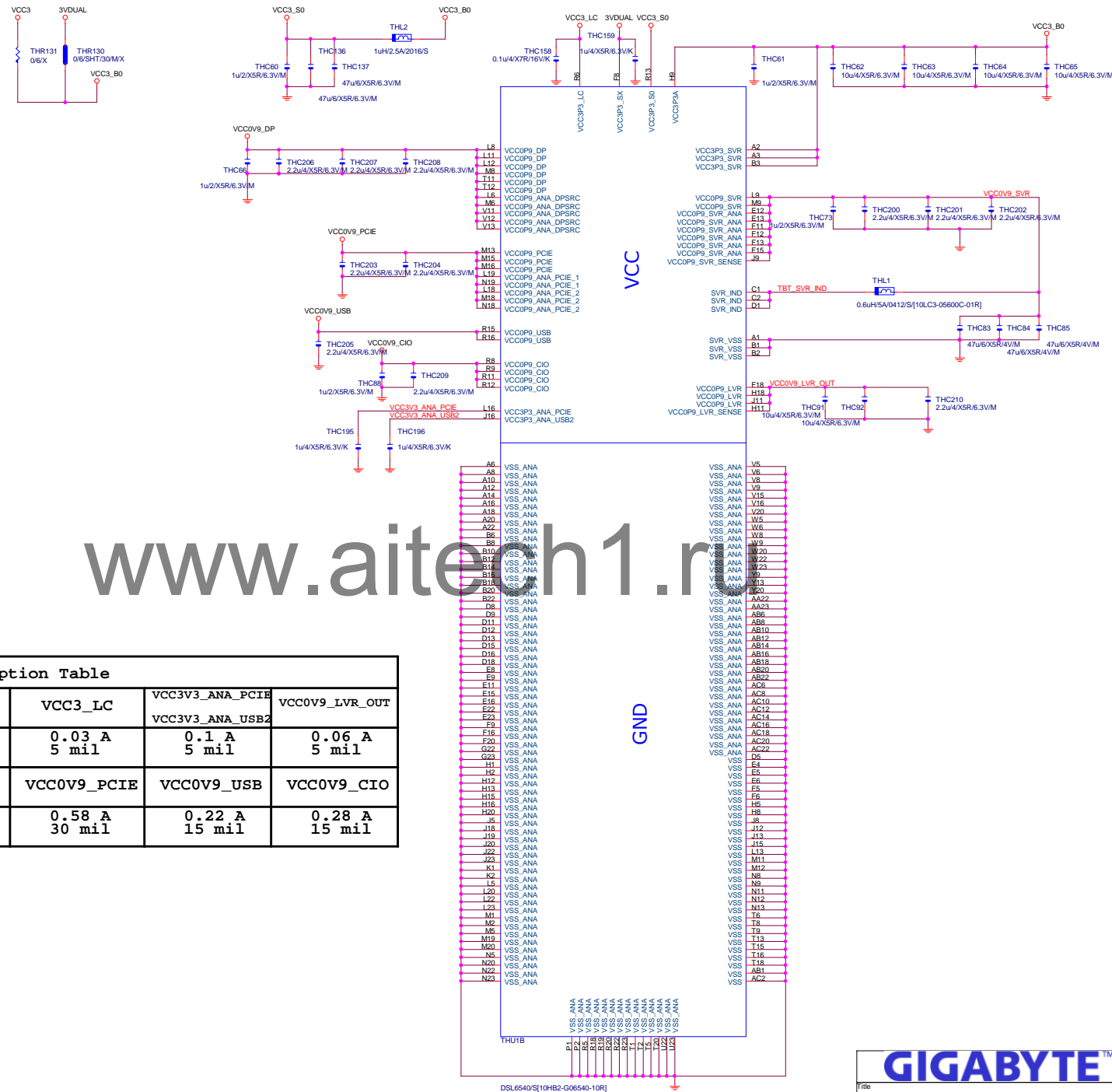
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Title			
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Size	Document Number		Rev
A	GA-Z170X-SOC Force		1.01
Date:	Wednesday, September 30, 2015	Sheet	80 of 88



INTEL AR USB31 module SCH 0.61 (2015/06/15)




Power Consumption Table

	VCC3	3VDUAL	VCC3_LC	VCC3V3_ANA_PCIE	VCC0V9_LVR_OUT
Max Current(A)	1.05 A 40 mil	0.19 A 10 mil	0.03 A 5 mil	0.1 A 5 mil	0.06 A 5 mil
	VCC0V9_SVR	VCC0V9_DP	VCC0V9_PCIE	VCC0V9_USB	VCC0V9_CIO
Max Current(A)	1.83 A 80 mil	0.7 A 30 mil	0.58 A 30 mil	0.22 A 15 mil	0.28 A 15 mil

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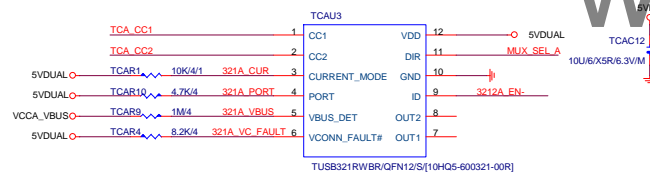
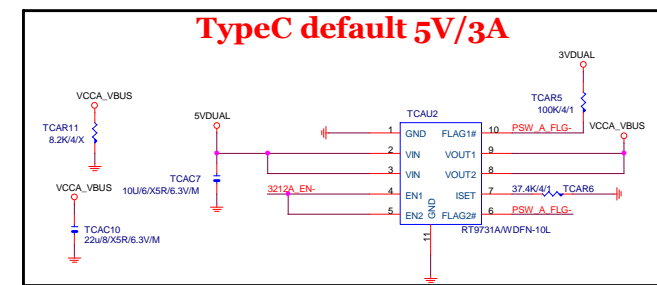
ALPINE RIDGE POWER		
File	Document Number	Rev
C	INTEL AR USB31	1.01
Date:	Wednesday, September 30, 2015	Sheet 82 of 88

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Title			
Type C port A			
Size	Document Number		Rev
Custom	GA-Z170X-SOC Force		1.01
Date:	Wednesday, September 30, 2015	Sheet 83 of 88	

* 0612



MUX_SEL
H - TypeC plug position 2
L - TypeC plug position 1

L - Default current / Pull down to GND or NC
M - Medium (1.5A) current / Pull up to VDD 500K
H - High (3.0A) current / Pull up to VDD 10K

NC - Dual Role

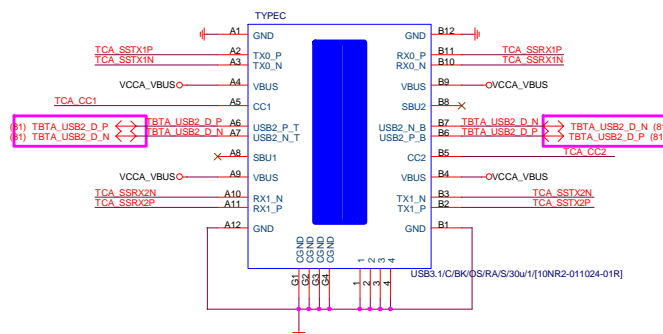


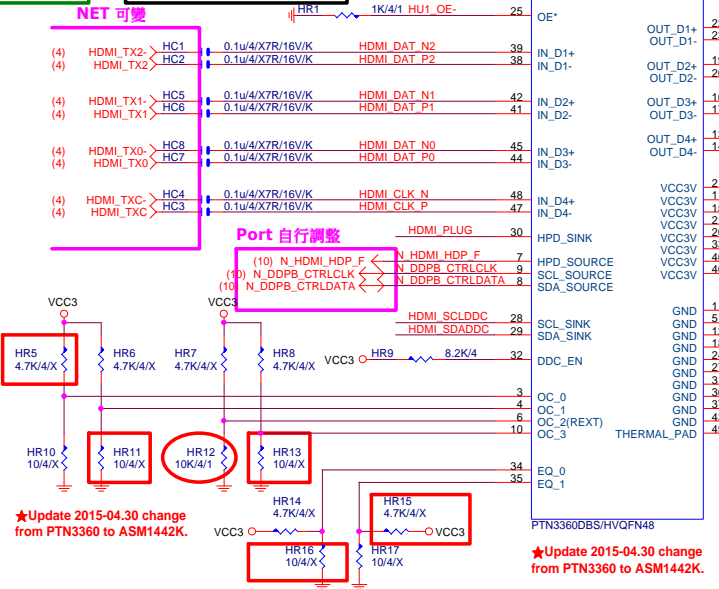
Figure 10: USB3.1 TypeC SCH. The figure shows three circuit diagrams for USB3.1 TypeC connectors. The left diagram shows a USB3.1 TypeC connector with pins 10, 9, 8, 7, 6, 5, 4, 3, 2, 1. The middle diagram shows a USB3.1 TypeC connector with pins 10, 9, 8, 7, 6, 5, 4, 3, 2, 1. The right diagram shows a USB3.1 TypeC connector with pins 10, 9, 8, 7, 6, 5, 4, 3, 2, 1. The diagrams are labeled with pin numbers and connector types.

For USB3.1 TypeC SCH

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Title			
TI TUSB321			
Size C	Document Number	Rev	
	INTEL AR USB31	1.01	
Date:	Wednesday, September 30, 2015	Sheet	84 of 88

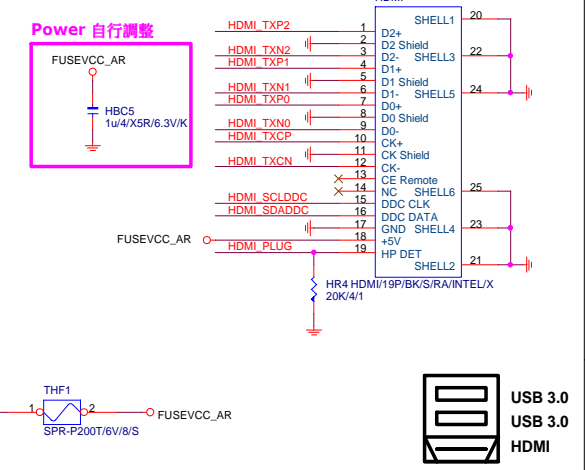
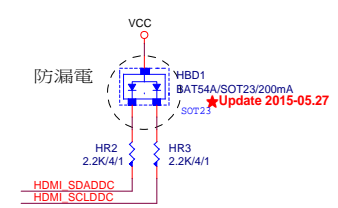
HDMI LEVEL SHIFT



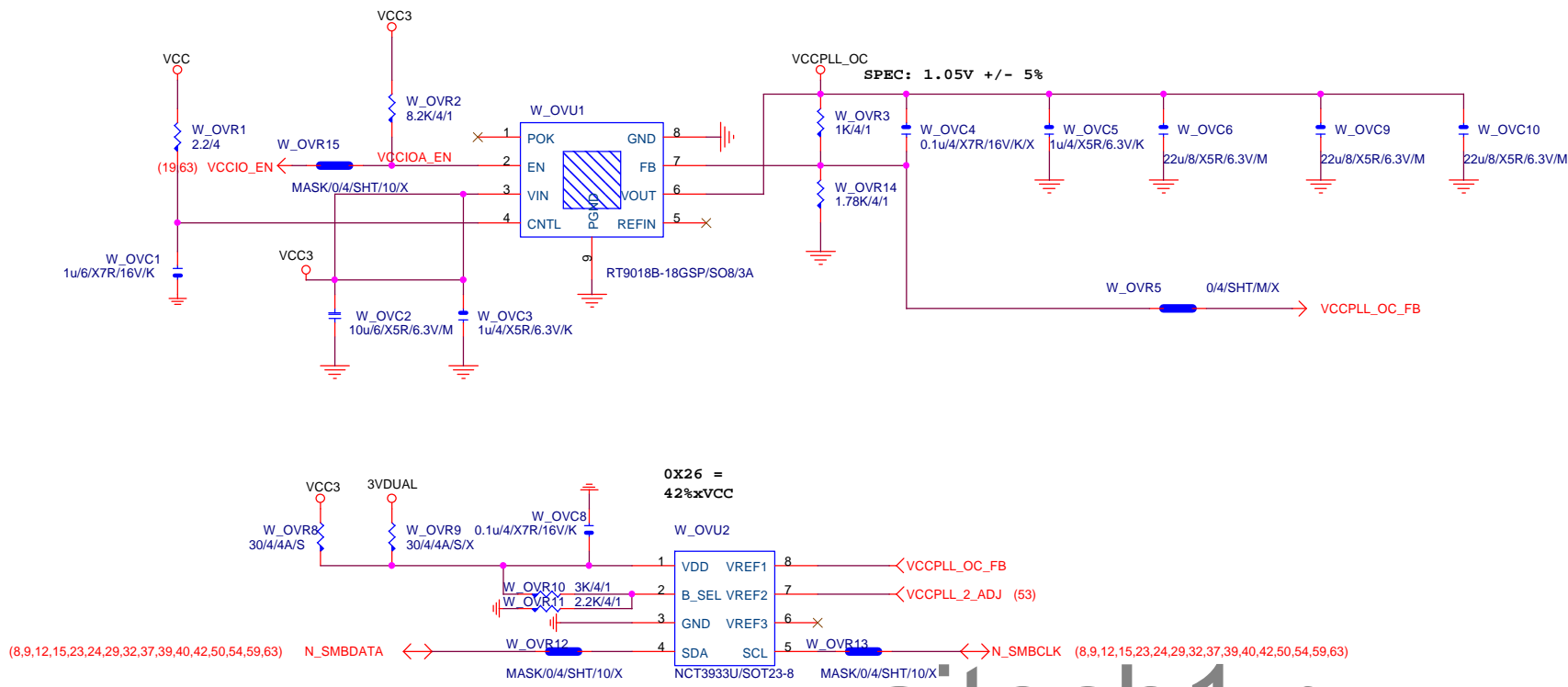
PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K
ASM1442:紅色框要上,HR12:3.16K

【技術通報R&D技術通報150】
HDMI eye diagram1.4版(deep color)會fail
原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL DOWN電阻)

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Title			
HDMI, R_USB30			
Size	Document Number	Rev	
Custom	MODULE	1.01	
Date:	Wednesday, September 30, 2015	Sheet	85 of 88



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8792

SIO

PCH

RS_PCH	ECRS_PCH
<input type="checkbox"/>	<input type="checkbox"/>

YRT1 close YQ1

VCORE_VS 盡量靠近CPU

VCORE_VS 盡量靠近MAEC4

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HS

Size	Document Number
Custom	

GA-Z170X-SOC Force

Rev	1.01
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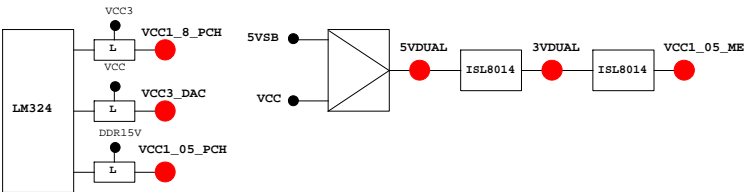
Date: Wednesday, September 30, 2015 Sheet 87 of 88

PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKT0CC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSI0	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PWRST1	
PCIRST1#/GP12	-PWRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBD_R	SEC_PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBD_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：

